Trends in RF & Wireless Packaging

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Abstract

This paper overviews the RF&Wireless packaging trends and introduces the four major impact areas Methodology and systems modeling , Board, assembly and housing, Prototyping, processing and production, Characterization on hand of real life examples. As an outview the major present trend of heterointegration and the picture of packaging waves is used to look into near future.

INTRODUCTION

In an age of borderless communication, with ubiquitous networks using multifunctional terminals and numberless services on the Internet, system hetero-integration and packaging technology plays a crucial role. Access to private and business data from any place in the world merges with various forms of electronic assistance in everyday life. In this context, system complexity and functionality are increasing, taking in everything from RF front-end over signal processing and storage to sensors and actuators, all in a functional system housing with integrated energy sources.

Universal mobile self-configurable electronic assistance terminals are the cornerstones of this development for the future. Small wireless and self-sufficient RF-modules (e-grains, electronic dust), linked by means of software interconnects, form the backbone of a sensing and actuating system in a near body, automotive or domotic environment. This trend presents a challenge for the entire spectrum of system development technologies.

RF & WIRELESS SYSTEMS INTEGRATION

Extraordinary advances have to be made in the areas of hardware and software development. Miniaturization is a basic prerequisite for bringing this vision of ubiquitous systems into reality. Body area and micro networks, together with e-grains and smart dust, could turn out to be an important element of this vision. Since packaging currently contributes up to 90% to the total component cost, industries are interested in identifying possible cost reductions while maintaining or improving functionality and reliability and ensuring volume production demands can be met. According to technology forecasts, packaging costs have to be drastically reduced using methods and processes which are suitable for automation [1].

While bandwidth and reliability are the main drivers for the long-haul market, size, flexibility and especially cost are the key factors for the Metro market of RF & wireless system modules. RF&wireless packaging needs to encompass all four steps of system integration:

Methodology, conceptual system development and modeling

Mechanical, thermal and electrical simulation is carried out in order to optimize the package architecture of RF systems (Fig.1), improve the selection of materials and estimate the lifetime. Thermal and thermo-mechanical simulation tools are used to optimize the cooling geometry and total package construction.

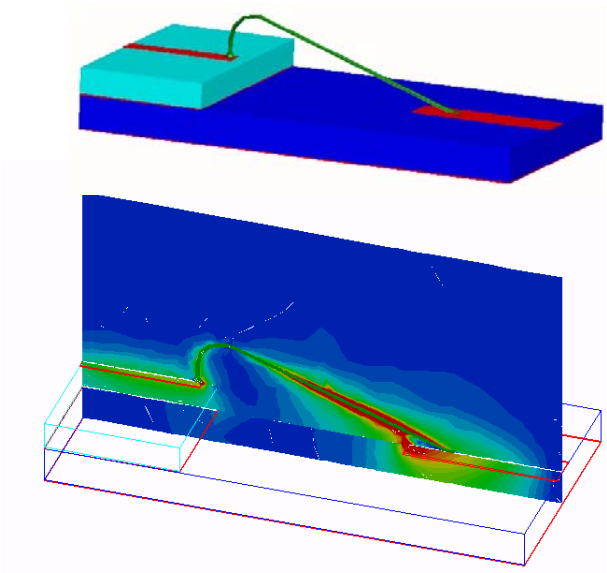

Fig.1: Example: EM-Simulation Wire Bond Interconnection (Ball/Wedge):

The system board of the future has to be high speed and RF compatible. Modern digital components tend to run at increasingly high clock frequencies (>1 GHz). Heterointegration urges the system designer to combine digital, analog and RF components in a single system and to shrink down the geometry in such a way that Systems are

integrated On a Package environment (SOP). This trend is continued in near future to Systems integrated On Chip combining sensors, actuators, MEMS and signal processing together with interfacing logic circuits (SOC). It is necessary to employ improved modeling methods paying more attention to heterointegration and RF aspects and to support a more complex system design in terms of more functions integrated meaning that more inter-disciplinary problems have to be solved. Since in parallel to the increased complexity also the time to market has to be reduced with each new generation, research and development has to work hand in hand and system design methodologies need to pay attention to reduced development cycles. Therefore tools and models should also be selected in order to enable a rapid prototyping. In line with these trends, the research activities are presently concentrated on characterizing and modeling the RF properties of various assembly techniques in order to reduce parasitics and optimize the signal transmission characteristics. Special interest lays on different bonding techniques (Fig. 1) (wire bonding, flip chip, ribbon bonding, embedded chip solutions etc.) and on passive components (like resistor, capacitor, inductor, transformer, transmission lines etc.). Substrate technologies like LTCC and multi layer organic are compared with respect to their potential for RF application at present.

Board, assembly and housing

For an efficient production of stacked devices for high quality/small size applications (mobile phones, digital cameras,..), chip manufacturing processes of today need to be changed. To decrease the overall thickness of packaged devices, the die and interconnect thickness has to become smaller, which implies thin wafer & handling, smaller pitches and thinner layer processing becomes necessary. In the field of bumping technologies main focuses are on wafer bumping & flip chip techniques for compound semiconductors (Fig.2), similar to those used for silicon. Fluxless flip chip assembly is suitable for low loss RF interconnects.

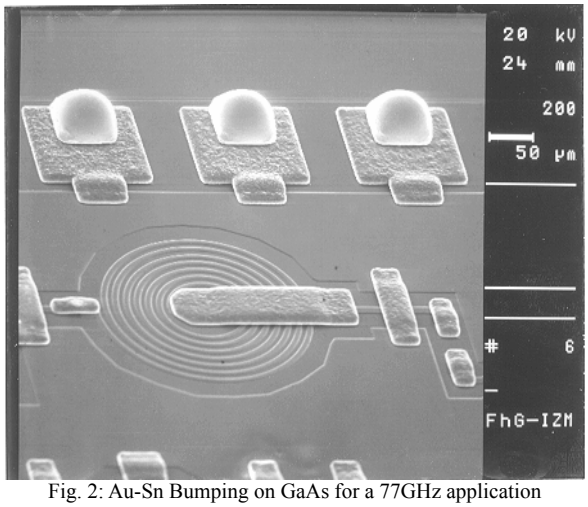

Fig. 2: Au-Sn Bumping on GaAs for a 77GHz application

Full wafer bumping or, for example, AuSn solder bumps with self-alignment contribute to the cost reduction of advanced RF modules. In the case of thinned semiconductors, the whole processing chain, from thinning equipment and processes to chip separation to the handling of thinned devices in logistics and assembly, has to be considered and optimized in terms of functionality and cost all the way up to the final system. Thinned semiconductor circuits offer a variety of advantages for RF&

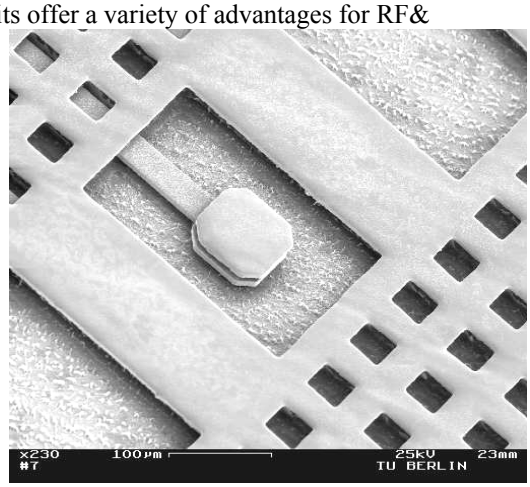

Fig. 3: REM-picture of a microstripline with gridded ground plane

wireless systems, including better cooling (performance), thermal management, 3D high density integration, flexible system modules [2,3].

Production capability on flexible substrates originally to be applied for transponders, smart cards, tickets, smart labels, wearable computing and smart clothes also becomes interesting for the development of high-functional mobile communication terminals, network cell stations and base stations. Thin film technology will provide impedance controlled wiring (Fig. 3) on top of sub-mounts or modules.

Polymer core solder balls could be an alternative method as bumping technique besides stencil printing and the use of preformed full metallized solder balls. The objective is the development of standardized components for RF applications up to 100 GHz. Therefore, it is essential to create a well defined gap between carrier and board. A polymer core solder ball consists of a large polymer ball coated by a Cu layer and covered with eutectic and/or high melting PbSn solder. The main advantage of such a system is the defined ball height after reflow. LTCC carriers with BGA contacts and daisy chain structures together with appropriate PCB boards were designed and manufactured as test samples. Two techniques were applied, on the one hand bumping with polymer balls and on the other hand a standard process with high melting PbSn solder as spacer. Under development is also to use polymer core solder balls with a diameter of 100 micron for flip chip bonding of Silicon chips on PCB boards at present.

For future electronic products more efficient system integration technologies are required to fulfill increased product demands like low cost, small size, multi-functionality and high reliability. Especially the gap in packaging density at system level between the high integrated circuits and the discrete components (which are mainly passives) has to be closed for future applications. Possible approaches to solve this problem is the thin film integration of the passives into the chip size packages of the integrated circuits or the arrangement of passives in integrated passive device structures.

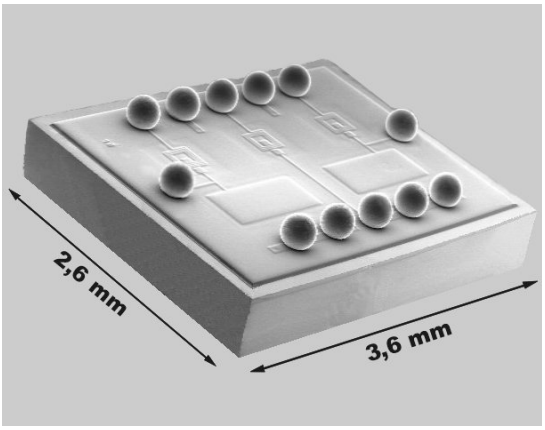

Fig. 4: Example Integrated Passive Device (IPD). This IPD is realized in a sixth layer Copper / Benzocyclobuthene (BCB) thin film built up on Pyrex. The low pass filters have cut off frequencies of 2,4 GHz for application in the Bluetooth band

But also on wafer level thin film integration of single passive components like coils, capacitors and resistors as well as passive filters and integrated passive devices (IPDs) is needed. By using these technologies steps not only single passive elements but also integrated passive filters for example at 2,45 GHz (Fig. 4)(bluetooth frequency) like band stop, band pass and low pass were realized. In the next step small chips including such passive filter structures and single passive elements could be realized for the use in a specific application. These integrated passive devices were solder bumped for flip chip mounting.

Prototyping, processing and production

In addition, speeding up of product design and development cycles ask for the development of rapid prototyping. Advanced tools and methods have to be combined with new production technologies. Wafer level packaging (Fig. 5), large panel manufacturing, surface mount technology and self-alignment and self-assembly processes, wafer level test and burn-in using standard equipment are just a few examples activities in this research field.

Another subject of growing interest in this area are methods for evaluating and optimizing high volume assembly, flexible substrate and board technologies and packaging and production processes on flexible substrates. This allows the combination of flexible semiconductor circuits, laminate mounted devices, polymer electronics and sensors and actuators with more conservative packaging and production technologies incorporated by a hetero-integration effort into advanced mobile RF modules [3]. Such an approach allows to add new functionality to state of the art technologies in a stepwise approach at lower risk for reliability and technology investment budget.

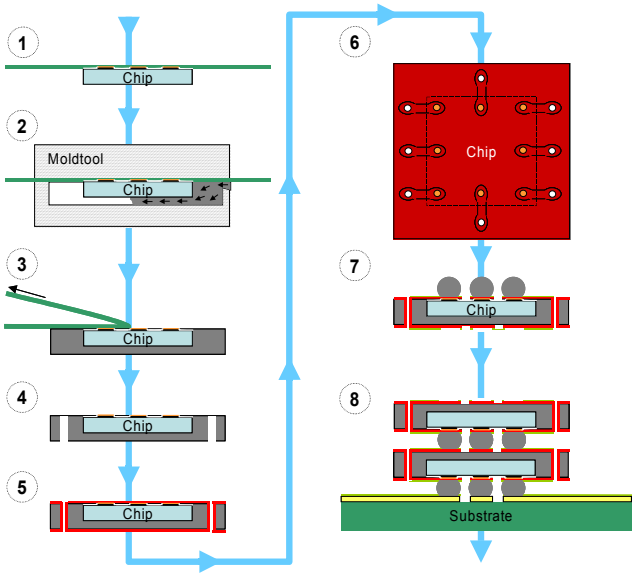

Fig. 5: Example WLP/MID Stacking Approach – Process Flow for Chips. A similar process is available for integration of passive or other discrete components onto a chip by WLP before performing the above process.

Characterization, test, reliability and preparation of certification

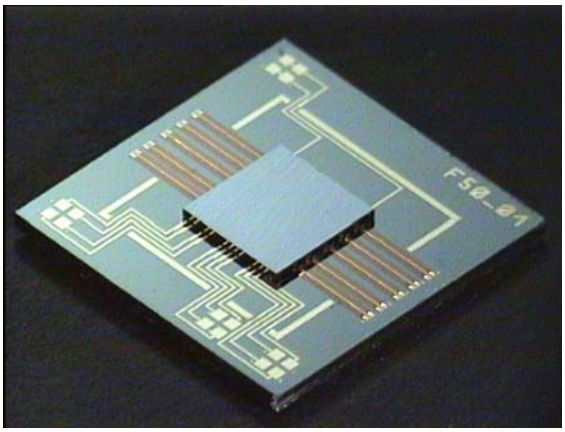

Fig. 6: Example of RF test modul for Au and AuSn bumping for a 77 GHz application. GaAs test chip (3.5 x 3.5 mm2) with coplanar waveguides in BCB multilayer thin film; Si substrate with microstrip lines, electroplated bumps with 30 and 50µm diameter. Measurements: Daisy chain, Four-point-Kelvin, RF characterization up to 77 GHz. Chip interconnection technology: TC bonding and AuSn reflow soldering

Microwave measurements are performed for RF and wireless package development (Fig.6), for modeling and outgoing process control, engineering verification, production screening and for various troubleshooting steps.

A Vector Network Analyzer (VNA) is commonly used for the system as well as active and passive RF components characterization yet additional components such as probes, manipulators and a probe station are required to extend the VNA capability for testing planar devices under test (DUT). The RF measurement system have to be calibrated before any measurements to avoid systematic errors and to increase the accuracy of the DUT characterization. Testing PCB boards with higher RF signals is often difficult. Special test fixtures are expensive and not flexible. Probe tips are often derivates from RF wafer probes and the dimensions are not done for PCB dimensions. These different sizes between the probe contacts and the signal layers on board often cause mismatch. For this purpose advanced test substrates have to be manufactured and applied during system development (Fig. 6). Reliability tests and failure analyses need to be used for package development in a wide spectrum of available methods. For example, for the full system evaluation and qualification, all necessary equipment from the reliability (i.e. ESD, EMV) of functional equipment (i.e. network analyzer, bit error rate test) to failure analysis needs to be available to qualify the completely assembled RF & wireless modules.

FUTURE TRENDS

At present the principle of heterointegration of different technologies (Fig. 7) is leading to the best compromise in systems functionality and cost of ownership for higher functional RF&Wireless systems.

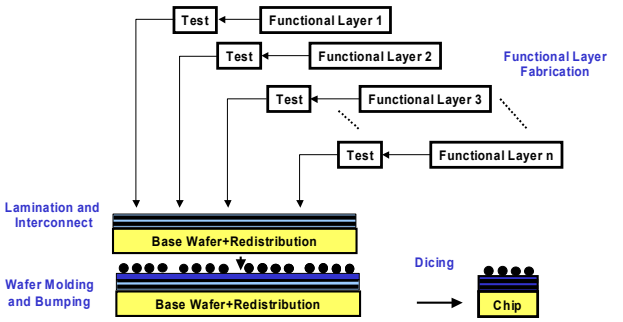

Fig.7: The principle of heterointegration of different technologies in a layer by layer approach leads to a cost effective merge of different component technologies enabling multifunctional systems.

Heterointegration requires a set of technologies like thinning of wafers and components, vertical system integration, functional layer technologies, assembly of thin components, thin interconnect technologies, wafer molding, bumping/ball placing and dicing. All these technologies need to be optimized and adapted in a modular integrated process flow. With such an approach packaging is acting as a systems integration carrier with the potential to reduce the packaging cost and to increase the functionality of a system at the same time. Several major technology trends for example the RF technology based ambient intelligence (body area, wearable computing, intelligent home, office and automotive environments, RFID) are based on RF & wireless systems. Some applications face a possible mass production in near future. A first step into these new system functionalities of an ambient intelligence is already visible in advanced mobile, PDA and notebook services and in the growing interest and application of RFID technologies. Communications over different RF links will be the backbone of such services. If a RF system will be produced in large volume suddenly the packaging cost becomes a very important area of cost optimization and a competitive factor. Therefore packaging technology needs to be regarded by RF&wireless systems engineers early in time and with more attention in near future. Looking to the history of packaging over the past decades a collection of packaging trends can be identified called packaging waves (Fig.8). At present the heterointegration wave is beginning and will be paralleled by a nano packaging wave in the near future. However, some of the nano aspects are already subject of todays R&D.

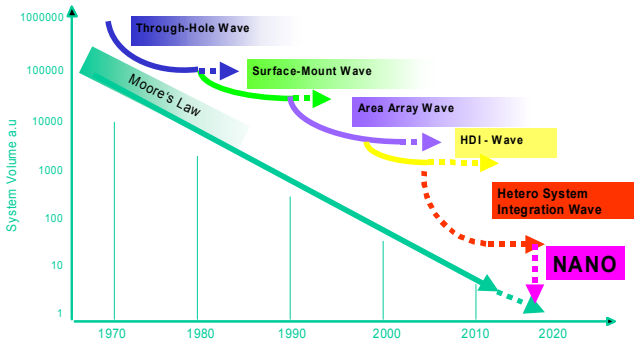

Fig. 8: The history of packaging in short: Major packaging efforts are the so-called Packaging Waves. High-Density Inteconnect and the Heterointegration efforts are the presently most important waves.

CONCLUSIONS

This presentation provides an overview to the scope of RF & Wireless packaging. On the hand of examples the steps and challenges of RF & wireless packaging is visualized and the development and present research topics as well as future trends are addressed.

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