RF SiP Technology: Integration and Innovation

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Abstract

With the continued demand for electronic systems and sub-systems with more functionality, higher performance, smaller size and lower cost, system-in-package (SiP) modules have been growing rapidly in recent years as an alternative solution to system-on-chip (SoC). As a packaging technology platform, SiP allows a high degree of flexibility in the package architecture, particularly for radio frequency (RF) applications. RF SiP is an enabling packaging platform for wireless communication and data access, which allows the integration of digital integrated circuits (ICs), logic ICs and RFICs into a compact RF system, or sub-system, within a single module format using state-of-the-art manufacturing technology converged from IC chip and wire packaging and SMT assembly.

In this paper, the trends of wireless access and mobile networking technologies are reviewed. Technical challenges and constraints to wireless systems for handset and mobile access applications are discussed. The packaging technology choice, performance and cost trade-offs are presented using RF SiP as a packaging platform. Finally, new RF SiP technology formats are presented to provide an innovative solution, through integration, to meet the demands of miniaturization, performance and cost for wireless handset and other mobile products.

INTRODUCTION

With the emergence of multiple wireless applications, industry initiatives and activities have been targeted at enabling wireless access and mobile networking technologies. Diversified applications using various wireless technologies, such as wide-area cellular networks, personal communication systems and wireless local area networks, have created an increasing demand on handsets and portable internet access appliances, such as 3G cellular phones, PDAs and mobile PCs. According to Prismark's report (July 2002), the RF wireless market remains one of the most promising, most exciting and dynamic market in the world with 20% to 100% annual growth in the next five years.

With widespread consumer acceptance of RF and wireless applications, there is an ever-increasing demand for electronic systems and sub-systems with more functionality, higher performance, smaller size and lower cost. These requirements translate to higher level microelectronic packaging challenges.

There are three major wireless network technologies: wireless wide-area network (WAN), wireless local area network (LAN) and wireless personal area network (PAN). With the increasing demand on higher date rates, the wireless carrier operating frequency is continuously moving higher to provided greater information bandwidth. For example from 800 to 1900 MHz for mobile phone wireless communication, to 2.4 to 5 GHz for wireless LAN and wireless PAN. These higher frequencies increase the complexity of the system design and packaging technology requirements.

Most wireless systems are portable, which require small size and lightweight products for consumers. Besides the traditional difficulties inherent in RF design, system miniaturization requires a high level of system integration, which further complicates the RF system. In a high performance RF application, the situation becomes more difficult. The RF system may require unique devices, such as low-loss power amplifiers and high linearity RF switches. In most cases, these devices utilize compound semiconductor materials such as gallium arsenide (GaAs). It is difficult to integrate these RF functions effectively with silicon-based processes using SoC technologies because the compound semiconductor product has very different materials, processes, metal finishes and passivations.

One major difference from digital devices, RF systems are highly dependent upon passive components for matching, tuning, filtering and biasing. High Q and tight tolerance inductors and capacitors are especially prevalent in wireless systems. In a typical mobile phone design, the passive surface mount devices (SMDs) account for a large portion of the total components and system board area. The capacitor is the major passive component, accounting for 80 to 90% of the total passive count. For these passives, the capacitance value can be in the range of 1pF to 10nF. From these statistics, it is obvious that the passive components, particularly capacitors, need to be addressed in order to reduce system size and cost.

In addition, power devices require a much higher level of thermal management, which makes the package integration even more challenging. The use of low-thermal conductivity polymers as substrates for RF SiPs dictate that the overall systems design are carefully crafted to maximize thermal dissipation.

In summary, "smaller, better, cheaper" is the dominant paradigm in today's RF wireless market. Increasing system demands for higher frequencies, more functionality, smaller size and lower cost require design and package technology to move to a higher level of integration.

SIP, AN ENABLING TECHNOLOGY FOR RF MODULE

Over the last several years SiP has become a fast growing package alternative [1, 2]. In comparison to SoC technologies, SiP technology offers the following advantages:

- High flexibility of package architectures allowing designers to combine active and passive components from a variety of semiconductor technologies without impacting the IC design and chip fabrication.
- High performance by providing high-level integration for digital, logic and RF functions and passive elements; short interconnection to minimize the parasitic effects both in the chip / substrate interconnection and the package / system board connection.

- Low system costs by eliminating multiple packages for individual chips while leveraging the existing packaging and SMT assembly manufacturing infrastructure.
- Small size factor by providing a platform for the integration of active devices, integrated and embedded passives.
- Short time-to-market. The system design, tuning and debugging are done at the substrate level, minimizing IC mask set redesign and wafer fabrication cycle times. This reduces new product time to market.
- Suitable for a wide variety of devices and materials.

RF SIP TECHNOLOGY PLATFORM

A common SiP example, shown in Fig 1, involves substrate technology, interconnection technology, passive integration and SiP assembly.

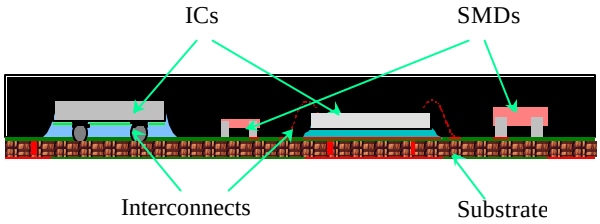

Fig. 1 Typical RF SiP platform

Substrate Technology. The substrate provides several features. First, it acts as the carrier to support the die and allow the die IO's to be distributed to the substrate and the package IO's. Second, it provides the interconnection and distribution of the signals and ground to various components and other die. Third, it may provide the ability to embed passives devices, such as inductors, capacitors, resistors, couplers, etc. and allow the use of controlled impedance transmission lines. Because of these functions, the substrate properties, material selection and process capabilities will directly affect the system performance. Different from substrates or interposers used for CSP or µBGA to pursue fine line/space for increasing I/O count, RF SiP substrates require low-loss metals and dielectrics to enhance the RF performance. These differences greatly limit the material selection and the substrate supply chain.

Laminate materials (resin with glass weave) are commonly used in RF SiP modules as the substrate material and offer a low cost solution for low to mid-range RF applications. The advantages of laminates include multiple metal layers for increased routing and passive integration, high-conductivity copper for low ohmic losses, large-scale laminate manufacturing processes for low cost and well-controlled metal definition for low pattern variation. Good dielectric core materials, thick metals, fine lines/spaces and small via hole areas, for z-axis interconnection between metal layers, are critical for RF applications. Current industry process capabilities can achieve line/space/thickness/via-diameter of 100/100/34/200 µm with relative ease. For further size reductions and higher packing densities, high density interconnect laminate technology (HDI) has been developed and put into large-scale production for RF SiPs in recent years. This technology further improves minimum lines/space and via features. The line/space/thickness/via-diameter of 75/75/25/75 µm is readily available in production capability. Unfortunately current laser drilled blind via technology results in a noticeable via holes in the exposed surface, which limit wirebonding and SMD in these areas. Future blind vias will be manufactured with full copper plating, yielding a smooth copper surface, further increasing the packing density on the top metal.

LTCC technology is a multi-layer, cofired ceramic process. As with most microelectronic grade ceramics, LTCC has lower dielectric losses and better dielectric and thermal properties than most laminates. The multiple layers allow passives to be embedded, improves routing capabilities and provides the ability to form cavities for bare die. Adding heat sinks to the cavity structure provides excellent thermal management for high power devices. This technology provides extremely versatile options for mid to high-range RF wireless applications. However, there are inherent disadvantages, which restrict LTCC from wide acceptance in RF SiP products. For example, high percentage substrate shrinkage during firing results in pattern registration issues, which require additional assembly attention. Relatively high ohmic loss metals, which require binders for adhesion to the ceramic, cannot compete with pure copper, Screen printed patterns have poor pattern repeatability particularly at fine lines and spaces. Long lead times for iterative designs can accumulate and severely impact time to market. Recent LTCC technology shows impressive progress: zero shrinkage LTCC, cofired copper-based metal conductors with etched features are available through some suppliers. Successful implementation of these technologies, with lower costs and cycle times, will help to increase LTCC in the RF SiP market.

Flex substrate technology is emerging in RF applications because of the advantage of high density interconnect capability, precision pattern processes and comparable RF performance with laminate and LTCC. The available process capabilities for line/space/thickness /via-diameter is 50/50/25/80 µm. Ultra-small, solid copper via plating capability is appearing in flex tape technology allowing reduction of the via diameter to 20~50 µm.

Micro leadframe technology has also made its appearance for RF SiP products. Without doubt, this is a new design concept for multiple die modules using the lowest cost substrate and assembly technology available. Confined to 1.5 metal layers, this substrate has limited interconnection and integration capabilities. Successful implementation of this substrate for complex SiP products requires passive integration elsewhere in the system, such as on the die or in an integrated passive device.

Interconnection. Wirebonding is still the dominant interconnection technology in RF front-end products due to the cost competitive and flexibility advantages over flip chip technology. In many cases wirebonds are used intentionally as integrated inductors of RF SiP devices. Conversely flip chip has other benefits over wirebonding. First, for RF products, the flip chip interconnect has the shortest electrical length and, therefore, exhibits lower electrical parasitic performance over a wirebond. Second, flip chip interconnects reduce overall laminate space by incorporating the interconnect vertically between the die and the substrate. Third, flip chip wafer bumping and reflow offer low interconnect variability allowing the system performance to be more predictable. Finally, flip chip assembly is compatible with SMD processes, which simplifies assembly by removing the chip and wire processes of die attach, epoxy curing and wirebonding. Fig. 2 shows GaAs wafer bumping and flip chip GaAs assembly implemented in ANADIGICS. Standard bump materials are solder (lead tin eutectic and leadfree) and gold. Recently the advent of solder-capped copper pillars has shown promise as an alternative to solder and gold. Unfortunately, the RF market shows a slow adoption of flip chip as a standard assembly tool due to cost. When compared to digital devices, RF IC's tend to have a low IO count, making it difficult to achieve cost-parity with wirebond costs per IO. Additionally high performance RF IC structures are based on compound semiconductor technology, such as GaAs. The die metal and finishing passivation differ than that of silicon ICs. Because of these differences it is difficult to take advantage

of the large wafer bump supply chain focused on serving silicon markets.

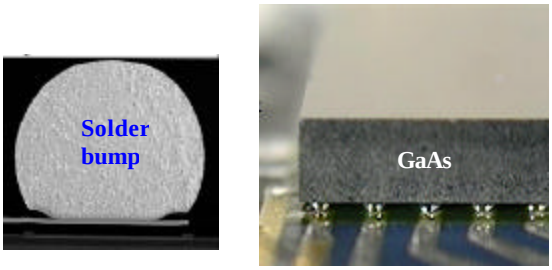

Fig. 2 GaAs wafer bumping and GaAs module assembly was implemented in ANADIGICS

Another unique interconnect technology is termed a "no interconnect" or build-up technology. This technology embeds die into a specialized substrate with metal directly applied between the die and the substrate in place of flip chip or wirebonds. It provides an advanced platform with the shortest interconnect and lowest parasitics and allows for a high transmission frequency or system clock speed. This technology had previously been applied to MEMS packaging with MCM-D approach [3] by placing a die in an etched Si cavity. The concept was also applied to high frequency (up to 110 GHz) GaAs MMIC packages [4]. Recently Intel is extending this technology for high-speed microprocessors at clock speeds of up to 20 GHz [5]

Passive Integration is a key component for system miniaturization and cost reduction. Compared with the SMD components on the substrate, passive integration has the potential to offer increased reliability, lower cost, lower part count, space savings and better performance predictability. Two types of integration technologies are used or being developed for RF SiP applications: integrated devices and embedded passives.

Integrated passive devices are based on thin film technology. Previously this concept was incorporated into the module substrate, termed MCM-D [1,6]. Because of the high cost and single side metal connection, MCM-D was not widely accepted in the low-cost, high-performance market as a substrate technology. Recently it is getting more attention as a stand-alone integrated passive device to reduce the SMD count in RF applications. Generally silicon-based thin film passives lend themselves more toward replacing SMD capacitors and resistors, but generally have inferior performance over SMD inductors due to their low Q-factor. By leveraging the wafer level deposition and lithographic processes, thin film capacitors and resistors show good electrical tolerance and provide an acceptable range of value with proper selection of materials and processes.

Another trend is to selectively integrate the passives on an active die used in the RF product. This allows existing areas to be reused. One example is to add a copper redistribution layer over the active surface to build up structures such as spiral inductors.

Embedded passive technology integrates the passive devices into the system substrate. This technology can be implemented by various methods: thick or thin film on a ceramic board (MCM-C), printing or etching patterns on an organic substrate (MCM-L), etc. As mentioned previously, LTCC is another method that allows a high number of passives to be embedded into the substrate. With high layer counts, high dielectric constant and thin ceramic tape, capacitance density of 5~200pF/mm^2 are achievable. However, screen-printed metal patterns exhibit poor dimensional stability and lower process tolerances. This directly impacts the capabilities of the RF system performance and may limit the device application. Laminate and flex are suitable to embedded inductors due their inherent low loss using copper metal. However embedded capacitors on laminate substrates suffer from low capacitance density, low resistance values and poor tolerances. There continues to be research and development in this area from academia and industry, such as George Tech [7~9] and the Advanced Embedded Passives Technology ("AEPT") Consortium in US.

RF SiP requires the use of a wide range of passives, particularly with capacitors. There is no one material or process technology which can provide a complete solution at an acceptable price. Technology selection will depend upon a tradeoff between process capabilities, passive performance and cost demands.

SiP Assembly is a convergent technology from microelectronic packaging and SMT assembly. It leverages worldwide subcontractor supply chains from both manufacturing technologies. The major assembly process steps include solder paste print, SMD pick & place, reflow, die attach, wirebond, encapsulation and singulation. With flip chip technology, the substrate metal finish requires lower gold costs than that of wirebondable gold. The successful development of overmold underfill will allow flip chip SiP to be cost competitive with standard chip and wire.

RF SIP FOR SYSTEM OR SUBSYSTEM INTEGRATION

An RF SiP packaging platform provides a wide range of technology selections. In today's RF integrated wireless designs the die, assembly and packaging are all interrelated and part of the whole. They can no longer be viewed as being independent of one another. The system-level approach, optimized for performance, miniaturization and cost on a diversified technology base becomes critical to the success of the RF SiP product development.

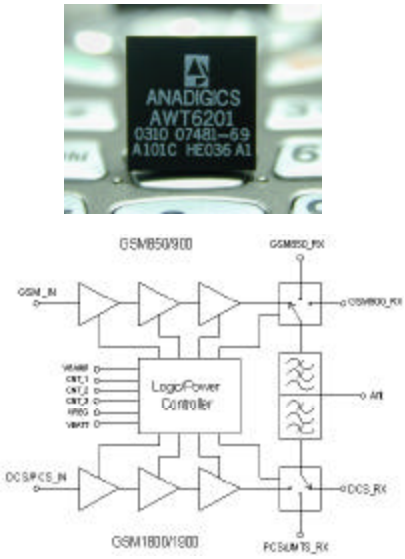

Fig 3 Highly integrated AWT6201 PowerPlexer™ in ANADIGICS

An RF SiP Testament. The quad band GSM PowerPlexer™, shown in Fig. 3, is a highly integrated RF module. It was the first in a new family of integrated RF modules for GSM/GPRS wireless handsets and introduced, by ANADIGICS, in 2003. The AWT6201 PowerPlexer™ integrates two dual band power amplifiers to support GSM850/900/1800/1900, power control circuitry, harmonic filtering and RX/TX switching in a single package. This SiP module simplifies the handset design process

by providing the handset manufacturer a single RF transmit module which requires zero RF tuning and optimization. The AWT6201 PowerPlexer™ combines 2 GaAs HBT die for power amplification, 2 GaAs pHEMT die for high speed switching, 1 quartz die for integrated passives and 1 silicon CMOS control die into a single 10mm x 11.0mm outline.

RF SIP TECHNOLOGY INNOVATION THROUGH INTEGRATION.

A novel RF SiP scenario, shown in Fig. 4, is presented here. The intent of this is to provide an innovative solution allowing higher integration, higher performance and lower cost for wireless handset and portable products. The technology options include:

- Integrated RFICs on a single compound semiconductor die solution for multiple RF functions.
- Wafer level redistribution technology for one, or more, thick Cu layers for high Q inductors and output matching circuitry.
- Wirebondable and solderable wafer finish metal provides an interface compatible with a wide variety of applications: chip and wire active die, passive die, SMD attach, etc.
- Multiple options of interconnection technology for design and process flexibility
- Unique thermal solution with an integrated heat sink
- High precision wafer-level substrate combined with low cost standard SMD and chip and wire assembly.

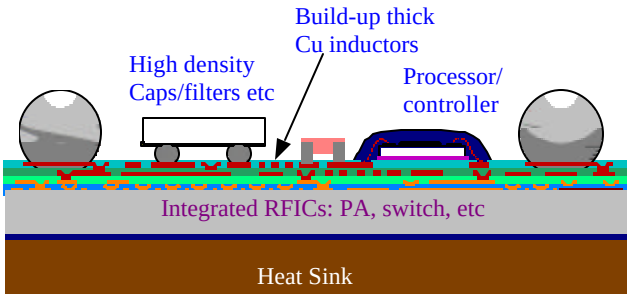

Fig. 4 Novel SiP scenario with overall integration

CONCLUSION

Over the last decade, information availability has expanded to everyone, anytime and anywhere, and is driving a communication revolution. The product requirements for such a diversified market shows an increasing demand on RF wireless electronic systems and sub-systems with more functionality, higher performance, smaller size and lower cost.

System-in-package (SiP) provides a new packaging platform with proven advantages of high flexibility, lower cost and faster cycle time than SoC. This technology enables integration of digital and logic ICs, RFICs and passives into a single module format with a cost-effective process.

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REFERENCES

[1] King L. Tai, “System-in-package (SIP): Challenges and Opportunities”, Proceedings of ASP-DAC 2000, Asia and south Pacific Design Automation Conference, pp. 191-196,

[2] Christopher M. Scanlan and Nozad Karim, “System-in-package technology, application and trends”, SMTA international Proceedings, 2001, pp. 764-773.

[3] W. Daum, W. Burdick Jr., and R. Fillion, “Overlay high-density interconnect: 1 chips-first multichip module technology”, IEEE Computer, Vol. 26, No 4, pp. 23-29, 1993.

[4] G. E. Ponchak, Chapter 9: “GaAs MMIC Packaging, GaAs MMIC Reliability Assurance Guideline for Space Applications”, NASA JPL Publication 96-25, 1996.

[5] Ravi Mahajan, Raj Nair, Vijay Wakharkar, Johanna Swan, John Tang and Gilroy Vandentop, “Emerging Directions For Packaging Technologies”, Intel Technology Journal, Issue 2, 2002

[6] Alastair Trigg, “Passive components for multi chip modules”, IME Newslink, July 1998.

[7] Sidharth Dalmia, Woopoung Kim, Sung Hwan Min, Madheavan Swaminathan, Venkatesh, Fuhan Lui, George White,

[8] Rao Tummala, “Design of embedded high Q-inductors in MCM-L technology”, Microwave Symposium Digest, 2001 IEEE MTT-S International , vol.3 2001, pp. 1735 –1738.

[9] S. Dalmia, J.M. Hobbs, V. Sundaram, M. Swaminathan, Seock Hee Lee; F. Ayazi, G. White, S. Bhattacharya, “Design and optimization of high Q RF passives on SOP-based organic substrates”, Electronic Components and Technology Conference, 2002. Proceedings. 52nd , pp. 495 –503, 2002.