Very Large Scale Electro-optical Device Process and Yield Challenges

Aviram Feingold, Daniel Majer, Arnon Arbel, Andrey Grinman, Marc Altman, Jeff Levy, Eyal Shekel

Chiaro Networks LTD, 5 Nahum Hefzadi St., Jerusalem 95484, Israel, afeingold@chiaro.com, 972-2-6595539

Keywords: GaAs, waveguide, yield, switching time, stress, TE/TM ratio.

Abstract

We report on the fabrication of a high yield very large-scale electro-optical GaAs-AlGaAs waveguide device, consisting of 18 beam deflectors with 128 waveguides in each deflector. The waveguides and n-type ohmic contacts are connected via 2508 bumps to a ceramic carrier, using flip chip technology. The carrier is also used as an optical bench for the optical components.

INTRODUCTION

We have successfully developed a set of processes that enable the production of a very large-scale electro-optical GaAs device with 2304 waveguides.
Four of these devices are used in an optical switch module (OSM). The optical switch module (OSM) is a complete 64x64 nano second switching time non-blocking optical switch.

Each device has 18 electro-optic beam deflectors, operating on the principle of optical phased array [1]. Optical phased arrays are a direct functional analog of microwave-phased array antennas used in RADAR systems [2]. The architecture of 2304 waveguides in a 12X30 mm chip requires yield improvement methodologies, which are usually not required for III-V optical semiconductor manufacturing. The epi layers in the device are 4.7 µm thick. A typical defect density for such a structure grown by MBE is 30 defects/cm^2. A typical defect density value of a similar structure grown by MOCVD is 5 defects/ cm^2 (defect > 1 µm size).

In order to achieve high yield devices, defect density lower than 0.6 defects/ cm^2 is required.

Apart from the low defect density challenge, other challenges have to be achieved in order to ensure optimal optical performance of the chip. These include good electrical connection and low stress post mesa etch processes.

Waveguides contact resistance I-V measurements are performed at early stages of the device fabrication. Good correlation is found between contact behaviour to switching time behaviour of the OSM. Switching time behaviour of the OSM is defined as the time it takes to switch from one optical output to another using the same input defelctor. Electrical measurements are used to predict switching time that can be measured only after the OSM is fully assembled. Obviously this has a huge impact on cost and OSM yield since assembling the complicated OSM is expensive and time consuming and should only be done using perfect chips. Waveguide definition and post mesa low stress processes are used in order to minimize stresses on waveguides. Stress on waveguides couple light from TE polarization to TM and excite higher-order optical modes, both mechanisms degrade device operation and consequently the OSM parameters.

Electrical measurements during wafer fabrication is a common methodology in Silicon devices fabrication, as process flow in such processes may include more than 20 lithography masks. In this paper we present processes and electrical testing procedures that facilitate high yield production of very large-scale GaAs electro-optical devices.

LOW DEFECT DENSITY WAVEGUIDES DEFINITION

Waveguide definition is the key process for achieving high yield devices. For this reason, instead of the commonly used TiPtAu p-type ohmic contacts, defined by a lift off process, a metal stack of Ti-Al-Ti is evaporated and then dry etched, using an ICP-RIE dry etcher.

Figure 1 shows SEM X-section of waveguide after mesa etch and Si_3N_4 CVD deposition.

Wafer yield is calculated using the following equation:

$$Y = Y_0 e^{-AD}$$

Where:

A = chip area

D = Defect density of process.

The 18X64 device area is ≈3 cm^2; thus the defect density required for at least one perfect device per wafer (six devices fit a 3” wafer) should be lower than 0.6 defects/ cm^2

As neither MBE nor MOCVD techniques can achieve such a low defect density, mesa process is

performed using a wafer with defect density higher by an order of magnitude (MOCVD) or two orders of magnitude (MBE) than the required defect density.

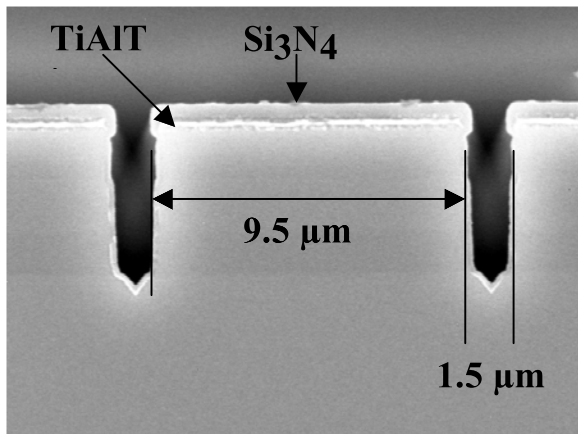

Figure 1: SEM image of 4.7 µm dry etching of GaAs/AlGaAs waveguides with Ti-Al-Ti P-type contacts and protecting Si_3N_4 layer.

A very slow and non-selective physical etch process, in which defects are etched with a similar etch rate of the EPI layers, was developed. Thus particles, which would otherwise short neighbouring waveguides, are etched away. A typical defect density of Chiaro's production wafer with MBE EPI layers is 0.1 defects/cm^2; and on wafers with MOCVD EPI layers the defect density is as low as 0.01 defects/cm^2.

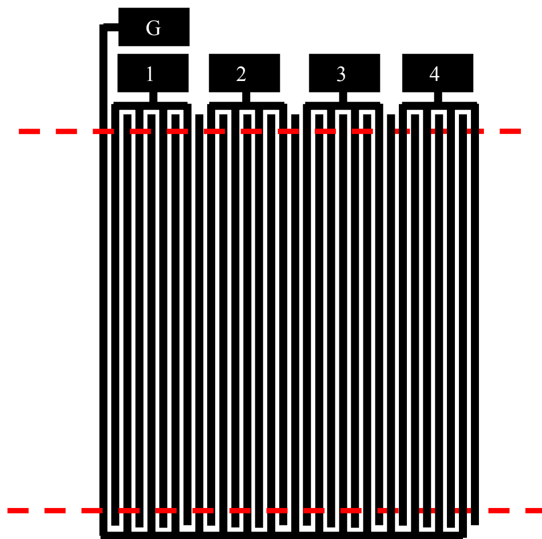

Figure 2: Scheme of a "Daisy Chain" structure. The structure is part of the device and is scribes away at the end of device fabrication process. The dashed red lines represent scribe lines.

We have designed a set of lithography masks in which electrical "Daisy Chains" are used to test structures that are part of the real device. Figure 2 shows a scheme of 32 waveguides connected into a Daisy Chain structure. At the end of the wafer process, these structures are scribed away living waveguides input and output facets.

In a real full 18X64 device, every 16 waveguides within a deflector are connected in a similar way and yield estimation of the devices is possible immediately after the Mesa etch process.

ELECTRICAL TESTS AND THEIR CORRELATION TO SWITCHING TIME

After the definition of waveguides and n-type ohmic contact, I-V measurements are performed, not only to find shorts between waveguides but also to predict switching time performance of the OSM.

Figure 3 shows switching performance of one input OSM channel (deflector) switching from one output fiber into another. As seen, switching time is about 20 nanoseconds. The router Chiaro builds requires switching time of less than 30 nanoseconds.

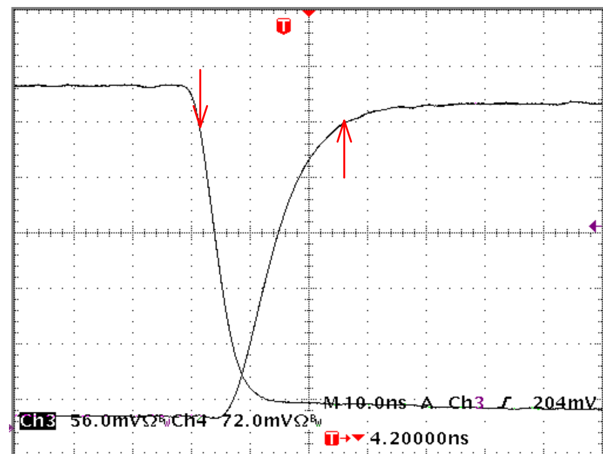

Figure 3: Switching time behaviour of the OSM. Light from a single input channel is switched between two different output channels. Switching time is calculated from distance between the two red arrows.

I-V measurement are taken in –30V to + 5V range. Analysis of the forward bias is relevant to switching speed prediction. Figure 4 shows the correlation between current at 1Volt versus device switching time. The plot is based on performance of six different devices, on which all waveguides were measured and an average current of each deflector at 1Volt was plotted. there are three different regimes in the graph: a) 0mA – 0.03 mA very sharp slope. b) 0.03mA – 0.25 mA – "knee" zone with moderate slope. c) 0.25 mV – 1 mV – linear line.

In order to assure a reliable device,a process engineer would define spec limits for such a device within the linear zone, above 0.25 mA.

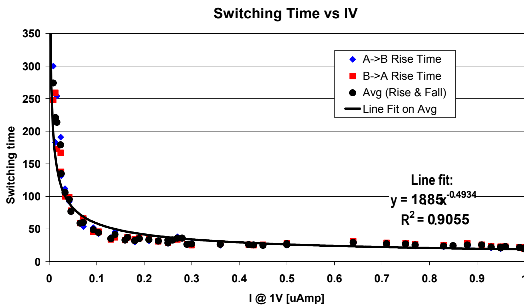

Figure 4: Correlation between current at voltage of one volt to device switching time. The plot is based on data from 6 devices (108 deflectors, 13,824 waveguides).

Figure 5 shows an I-V plot of a good contact, which is defined as a contact with break off voltage around 0.5 Volts and that reaches compliance current of 1 mA below 1V. Good devices, such as this one, shows no sensitivity of its I-V plot to lighting conditions. , In Problematic devices, e.g. with high contact resistance or with Schottky contacts, break off voltage and compliance voltage are increased and device shows high sensitivity to lighting conditions during measurement.

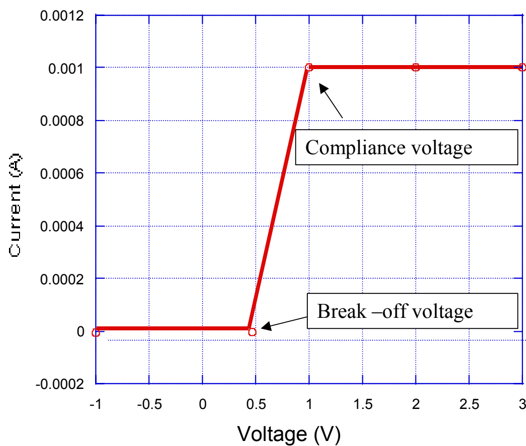

Figure 5: Typical forward bias I-V plot with break up voltage at 0.5V and compliance voltage at 1V

LOW STRESS POST MESA ETCH PROCESSES

After the post mesa etch electrical test, a Si_3N_4 layer is deposited protecting the waveguides from humidity and subsequent layer bridging problems. Dry etch process is used to open vias in the Si_3N_4 layer. These vias are used to connect the next metal pad layer to each waveguide separately and to n-type ohmic contacts located between the deflectors.

Next, N type ohmic contacts are defined between each of the 18 deflectors in the device (as is shown in Figure 6).

A real challenge is the bump connection to waveguides using processes that apply minimum stresses on the waveguides. Key parameters for minimum waveguide stresses in post mesa procedures follow. .Figure 6 shows the metal pad connecting bumps to waveguides. The metal pad is evaporated above a polyimide planarization layer, in which vias are opened above previously etched Si3N4 vias. Polyimide type, thickness, and curing conditions are important parameters for low waveguide stress.

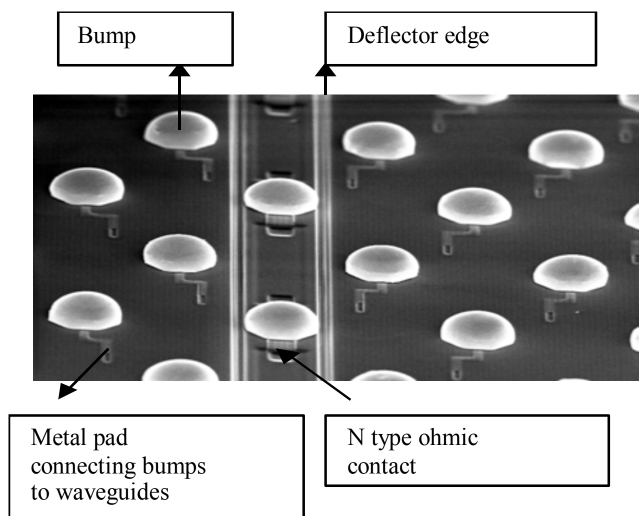

Figure 6: SEM of part of two deflectors with bumps connected to waveguides and to n type ohmic contacts placed at the spacing between deflectors.

Metal pad thickness and shape were also found as very important parameters. Above the metal pads a second polyimide layer is coated and large vias are opened and define bump bases (Figure 7). The second polyimide layer acts as a bump cushion reducing the stress to underlying waveguides. Under bump metalization, Ti(W), is sputtered to protect the wafer during electroplating and to enhance bump connection reliability. AuSn pillars are electroplated through a thick photoresist mask. The pillars are then reflowed into bumps and get a mushroom like shape with eutectic AuSn top and Au base (Figure 7).

Scribe and ARC coating on chip facets follows. A flip chip process is used to connect all 2608 bump to a ceramic carrier with Au pads. Both the reflow and flip chip process conditions have major effects in stresses on waveguides. It is helpful to define a quantity we call TE/TM ratio. It is the ratio in dB of the energy in TE

and energy in TM polarization at the chip output when pure TE laser light is inserted to the chip.

TE/TM ratio without implementation of the above procedures was as low as 2 to 4 dB. After implementation TE/TM ratio of 14 to 15 dB is achieved, repeatable both, within wafer and between wafers.

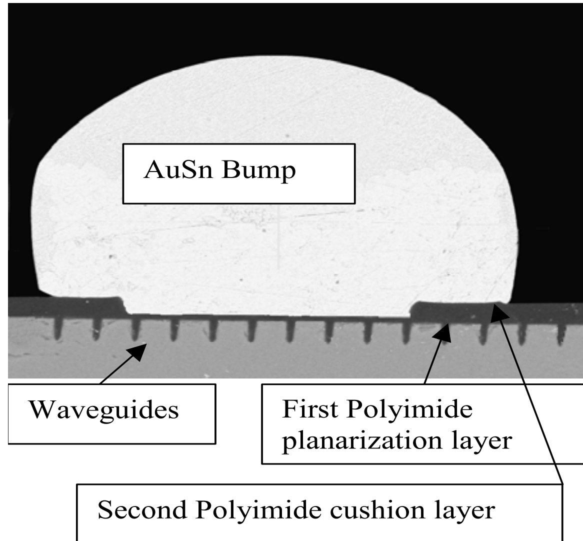

Figure 7: SEM X-Section of AuSn Bump sitting above waveguides (connection to waveguide not shown)

At this stage a ceramic assembly containing the flip chip device is again electrically tested for shorts between waveguides and across each waveguide P-N junction full I-V for each waveguide is performed. It is then transferred to the optical assembly line for further processing

CONCLUSIONS

We have developed processes and electrical test methodology that allow a very large-scale electro-optical device to be routinely manufactured with high yield. We have found and optimized process parameters, which affect Switch over behaviour and TE/TM ratio of the optical switch. The device has 2304 active waveguides and is flip chip assembled to a ceramic chip carrier. The ceramic carrier is also used as the optical bench in later fabrication processes.

REFERENCES

[1] P.F. McManamon et al, Proc. IEEE, 84, pp. 268-298 (1996)
[2] T.C. Cheston et al, in Radar Handbook, 2nd edition, Chap. 7, pp. 7.1-7.82 (1990).