Toward the Development of Hybrid MEMS Tunable Optical Filters and Lasers

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Abstract

There is strong interest in the development of tunable lasers and optical filters for a number of optoelectronic applications. From a telecommunications standpoint, compact, efficient, and *affordable* tunable sources and filters could find immediate widespread use for wavelength division multiplexing (WDM) systems, enabling incredibly dense optoelectronic communications over a single optical fiber. From a military standpoint, *robust* tunable sources would readily be inserted into platforms requiring fixed-wavelength optical pumps (such as for fiber amplifiers or atomic clock systems) or for hyperspectral imaging systems that require stable, pixilated filter elements.

INTRODUCTION

As emphasized above, "robust" and "affordable" are qualities that are often at odds with each other, and methods to implement tunable filters and emitters continue to be an area of active research and development. For instance, most WDM methods utilizing common edge-emitting lasers require complex biasing, demand system-specific optical coupling configurations, and are difficult to manufacture. This reduces system reliability, yield, and thus increases unit cost. In an effort to circumvent some of these issues, all-semiconductor tunable filters and diode lasers have been fashioned via micro-electro-mechanical (MEMS) electrostatic, thermal, or magnetic actuation (see, e.g. [1]). These devices typically employ a monolithically grown or deposited multi-layer mirror or reflector suspended by one or more flexures. A sacrificial layer of material is removed via processing using either wet or dry etch techniques, leaving behind a suspended reflector element connected to the base substrate via one or more flexures (see FIGURE 1). As the reflector is displaced, the effective optical path length is modified, thus tuning the device's fundamental resonant frequency. This method has been employed to create tunable vertical-cavity surface-emitting lasers, with beams that are naturally less astigmatic than edge-emitting structures, thereby reducing some costs incurred coupling the output beam to a fiber. Nevertheless, the processing steps of such devices are cumbersome, again increasing the price per unit beyond acceptable limits. This is further evidenced by the recent failure of companies using this technology to remain solvent.

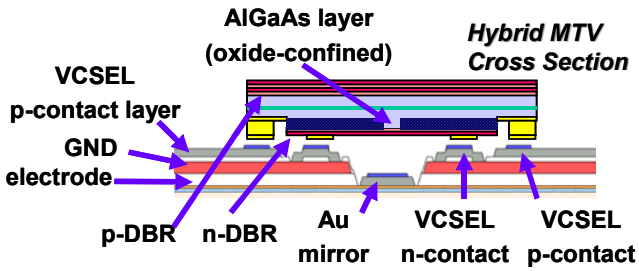


FIGURE 1. Schematic illustration of a hybrid MEMS-tunable VCSEL. The VCSEL is bonded via co-planar contacts. Tuning is achieved via coupled cavity resonances between the bottom Au mirror and a thin, low-reflectivity Bragg mirror on the lower part of the III-V structure.

More recently commercial and research institutions have more vigorously pursued a hybrid integration approach. The ability to match III-V emitters onto separately developed/processed MEMS structures is attractive for a number of reasons: Development cycles for transducers are typically much slower than CMOS, so when yield problems occur the hybrid approach allows discarding defective parts; the development of monolithic (i.e. all-semiconductor) systems is difficult and expensive, and an error in any portion of the structure ruins the entire device operation; moreover, many silicon MEMS design techniques, such as the use of dimples to prevent stiction, are not yet an option for most monolithically grown devices. Hybrid integration avoids these issues and mitigates risks by allowing one to separately optimize and tailor components' individual operations.

We highlight here our efforts to produce tunable filters and lasers, with operation centered around 980 nm. Our approach is somewhat novel in that we seek to attach III-V structures, such as a Bragg mirror, LED, or VCSEL, onto a MEMS foundry platform via flip-chip bonding. We utilize techniques in the MUMPS® foundry process to create gold mirrors of different "step heights" that allow tuning of coupled-cavity structures over various wavelength ranges (FIGURE 2). We illustrate many of the design criteria to consider in the creation of such hybrid devices. We also

demonstrate comparisons between simulations of such structures to measured results.

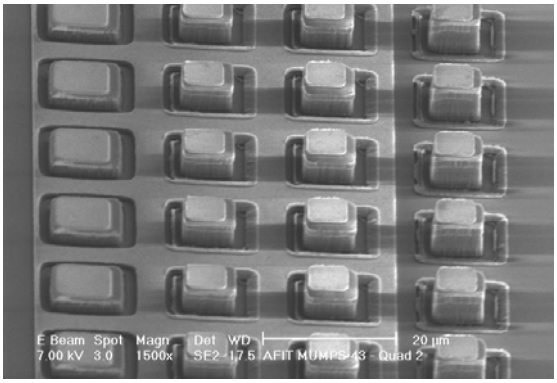


FIGURE 2. SEM image of vertically displaced Au central reflector test array formed in the MUMPS process.

The most formidable impediment to implementing this concept has been development of flip-chip bonding procedures that enable the hybrid devices to withstand subsequent sacrificial etch and release processing (see FIGURE 3). We describe below several techniques and materials attempted for hybrid integration, including metal-metal bonds and alloys, and the use of photoresists as flip-chip bondpad elements.

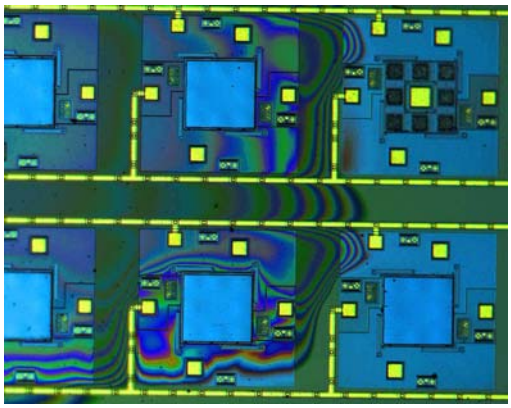


FIGURE 3. Microscope image of flip-bonded semiconductor material onto MUMPS® MEMS structures. Note the upper right device had the top Bragg reflector removed to show the underlying flip-bond pads of the MEMS device.

METHODOLOGY

The final step of the MUMPs® foundry process [2] to fabricate the MEMS actuators is the deposition of a thin chrome adhesion layer followed by 0.5µm of gold. For the purpose of our research, this gold has been patterned to form 50µm x 50µm bump bond pads on the surface of MEMS piston actuators.

Semiconductor DBR mirrors, consisting of quarter-wavelength layers of GaAs and $Al_xGa_{1-x}As$, were grown epitaxially via MBE on GaAs substrates. A thick AlAs deposition was grown between the substrate and the DBR mirror as a sacrificial layer. AlAs can be quickly etched away by an HF solution, thereby releasing the DBR mirrors from the substrate. The DBR mirrors are 250µm x 250µm and are defined using a sulfuric acid wet etch. Either gold, indium, or polymer bumps are deposited onto the surface of the DBRs and patterned by lithography into 50µm x 50µm bump bonds (FIGURE 4).

In order to successfully flip-bond relatively delicate DBR mirrors onto MEMS actuators, there is a trade-off space between bonding temperature, time, and pressure. In general, higher pressure increases bond strength, but also increases the potential for cracked and deformed mirrors. A higher bonding temperature and longer bonding time helps Au-to-Au and Au-to-In bumps form strong eutectic bonds, but high temperatures for extended periods may have negative effects on existing metal substrate components such as wire bonding pads, power lines, or MEMS structures. Therefore, recipes for each bump bond material must be optimized to increase bond reliability while reducing or eliminating the potential for damage to device structures.

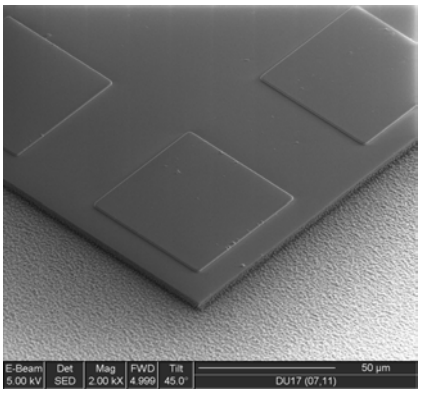


FIGURE 4. SEM of $GaAs/Al_{0.4}Ga_{0.6}As$ DBR mirror with 0.5µm Au bump bonds. Mirror is still attached to GaAs substrate by AlAs sacrificial layer.

Au-to-Au Bump Bonds

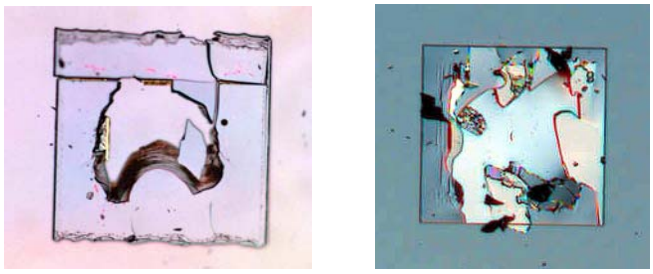
Before deposition of Au bump bonds, a 300Å chrome adhesion layer is evaporated onto the surface. Chrome is selected instead of the more common titanium adhesion layer due to its resistance to HF. Titanium is quickly etched away by HF and causes the Au bumps to detach from the semiconductor surface during the release process. 5000Å Au bump bonds, defined by lift-off resist lithography, are deposited over the Cr adhesion layer by evaporation or plating.

The advantages of gold bonds include strength, resistance to oxidation, and excellent conductivity. High conductivity is essential for a MEMS tunable VCSEL device, but not required for our MEMS tunable filter design.

A variety of flip-bonding parameters were attempted in order to find an optimal Au-to-Au bonding recipe. Temperature was varied from room temperature to 400°C, time was adjusted from 3 min to 60 min, and pressure from 166 kg/cm^2 to 1665 kg/cm^2. An optimal flip-bond recipe for reliable, strong Au-to-Au bonds was

achieved with a temperature of 375°C for 1 hr at 1333 kg/cm^2 (see TABLE 1).

At this combination of temperature, time, and pressure, 100% of the bump-bonds and DBR mirrors are successfully flip-bonded onto the MEMS wafer. Unfortunately, none of the semiconductor mirrors survive the flip-bonding process intact due to the high pressure endured during the bonding process. After bonding and release, mirrors are severely cracked and damaged (see FIGURE 5b). An attempt was made to strengthen the DBR mirrors by increasing the number of GaAs/$Al_xGa_{1-x}As$ quarter-wave mirror pairs from 17 to 25, and adding a 1μm thick GaAs buffer layer. This increased the thickness of the semiconductor DBR mirrors from 2.6μm to 4.7μm. The results were identical, and 100% of the thickened mirrors were cracked during bonding.



(a) (b)

FIGURE 5. GaAs/$Al_{0.4}Ga_{0.6}As$ DBR mirror (a) cracked during full-strength HF release process, (b) damaged by high-pressure flip-chip bonding (1333 kg/cm^2)

Au-to-In Bump Bonds

Due to the poor results obtained using Au bump bonds, indium bonds were investigated as a way to lower the bonding pressure. Indium is a much softer medal than gold, but forms a strong eutectic bond with gold at temperatures above 200°C [5]. Indium bump bonds can be evaporated or plated onto the semiconductor DBR mirrors, patterned using a lift-off resist, and flip-bonded to the Au bump bonds on the MEMS actuators.

The disadvantage of In-Au bonds vs. Au-Au bonds is reduction in bond strength and a decrease in electrical conductivity. In addition, deposition of indium bump bonds requires a more challenging fabrication process than simple gold bumps. First, a 300Å Cr adhesion layer, followed by 1500Å Au is evaporated on the semiconductor DBR surface. 15,000Å of indium is either evaporated or plated over the Cr/Au. Due to the extremely fast oxidation of indium, a 1000Å cap of Au is evaporated over the indium bumps. If the Au cap is not placed over the indium, the bumps should be ion-milled immediately before flip bonding to remove the layer of oxidation.

As before, flip-bond parameters were adjusted to find an ideal In-to-Au bonding recipe. Although indium and gold form a eutectic bond at 200°C, a higher bonding temperature was required to achieve reliable and repeatable bonding of the DBR mirrors to the MEMS actuators. A temperature of 275°C for 1 hr at 333 kg/cm^2 proved to be the best combination.

The Au-In bonds are not as strong or reliable as the Au-Au bonds, with only 73% of bonds intact after release. But the bonding pressure is much lower, and the semiconductor DBR mirrors survive the flip-bonding process intact (see FIGURE 6).

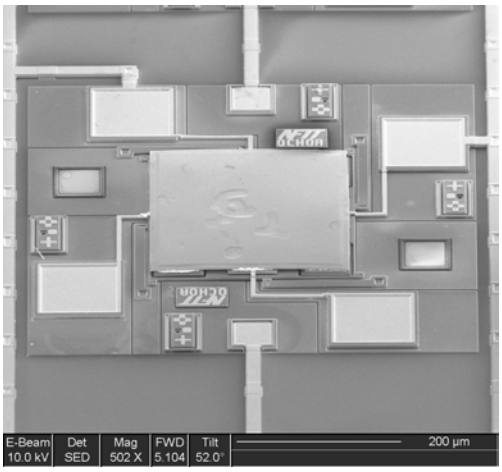


FIGURE 6. SEM of polysilicon MEMS (MUMPS®) actuator flip-chip bonded using In-Au bumps to a GaAs/$Al_{0.4}Ga_{0.6}As$ DBR mirror. Note damage to mirror occurred during rapid release in full-strength HF.

SU8-to-SU8 Bump Bonds

SU-8 2000 is a high contrast, epoxy based photoresist designed for micromachining and other microelectronic applications [3]. After exposure to near-UV and a post-expose bake, SU-8 is a highly cross-linked epoxy, which makes it extremely difficult to remove with liquid developers and solvent based resist strippers. In addition, it is highly resistant to most chemicals, including HF.

Initial testing indicates that SU-8 2000 performs well as a bump bond for flip-chip bonding. Using SU-8 2002, it's possible to deposit 1μm bump bond pads on both the surface of the semiconductor DBR mirrors and the MUMPs® MEM actuators. The SU-8 may be processed normally, including pre-expose bake, near-UV exposure, post-expose bake, and develop. The DBR mirrors may then be flip-chip bonded to the MEMS actuators with excellent results.

TABLE 1
FLIP-BONDING PARAMETERS

Bond Materials	Temp	Duration	Bond Pressure
Au - Au	375° C	60 min	1333 kg/cm^2
In - Au	275° C	60 min	333 kg/cm^2
SU8 - SU8	165° C	20 min	416 kg/cm^2

Flip-bonding at a temperature of 165°C for 20 min at 416 kg/cm^2 resulted in 100% intact bonds. In addition, all

semiconductor DBR mirrors remained intact and undamaged. Since SU-8 is not a conductor, this flip-bond recipe isn't ideal for MEMS tunable VCSEL devices, but it is a useful tool for the development of MEMS tunable filter designs.

Consequences of High-Temperature Bonding

Although In-Au bump bonds successfully attached DBR mirrors to MEMS actuators, there were unintended consequences of the high temperature flip-chip bonding (275°C). According to Burns [4], MUMPs® devices subjected to temperatures greater than 250°C for extended periods may suffer thermal damage. This damage only affects the gold, and may be due to a widening of the eutectic bond under the gold layer and/or the release of phosphorous from the polysilicon under the gold. The thermal damage appears as discoloration and loss of planarity in the gold layer. The resulting damage reduces reflectivity of the gold from 97% to 67%.

In addition, extended soaking of thermally damaged MUMPs® wafers in HF results in the lift-off of gold from the polysilicon surfaces. This includes all contact pads and wiring on the wafer surface, rendering the MEMS devices unusable.

Unfortunately, this was discovered late in the process development stage. It may be possible to achieve good flip-bonding results using In-Au bump bonds by modifying the parameters and lowering the bond temperature below 225° C. This will be explored in follow-up research.

Sacrificial Release Issues

Both the MUMPs® devices and the GaAs/AlGaAs DBR mirrors utilize HF to release their respective sacrificial layers (SiO_2 and AlAs). According to [2], 1.5 to 2 min in 49% HF will fully release a MUMPs® die. Experiments show it takes 5-6 min to fully release the MUMPs® devices and separate the attached DBR mirrors from their GaAs substrate.

Unfortunately, this release chemistry resulted in nearly complete destruction of every mirror during the release process (see FIGURE 5a). It was previously assumed that mirror damage was solely due to excessive pressure during flip-bonding. This was only the case when attempting the high-pressure Au-Au bond recipes.

It's hypothesized that turbulence and bubbles formed by the rapid etching of AlAs place excessive strain on the fragile GaAs/AlGaAs DBR mirrors. The result is cracking and destruction of the mirror, rendering the device useless.

A diluted HF solution consisting of HF:IPA:DIW (1:3:6), increases the DBR mirror release time from 5 minutes to 75 minutes and eliminates cracking of the DBR mirrors. After release of the GaAs substrate, the MUMPs® die must be placed in a full-strength HF bath for 3-4 minutes to ensure complete release of the MEMS actuators.

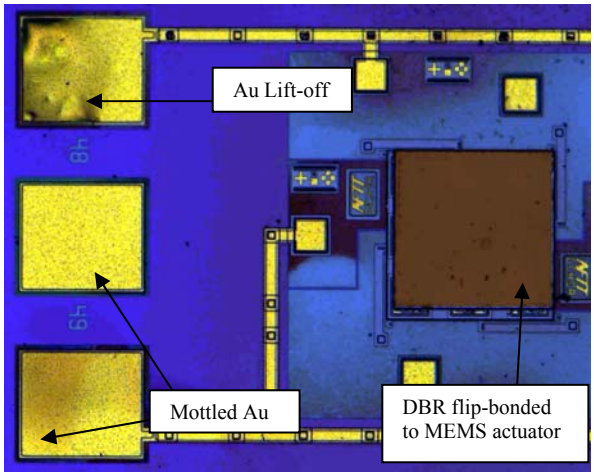


FIGURE 7. Thermal damage of gold due to high temperature (275° C) flip-chip bonding. Note lift-off of bond pad from MUMPs® substrate and degradation of gold.

CONCLUSIONS

We have made significant strides towards the development of a hybrid approach for the integration of III-V structures, such as a Bragg mirror, LED, or VCSEL, onto a MEMS foundry platform via flip-chip bonding. Considerable effort went into the development of flip-chip bonding procedures that enable the hybrid device to withstand subsequent sacrificial etch and release processing. In addition, release chemistries have been optimized to eliminate stress on fragile III-V structures. Follow-up research will explore lower temperature In-Au flip-chip bonding and expand research into polymer bump bonds.

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ACRONYMS

MEMS: Micro Electro-Mechanical System
MUMPs®: Multi-User MEMS Processes
PECVD: Plasma-Enhanced Chemical Vapor Deposition
MBE: Molecular Beam Epitaxy