Junction Temperature and Thermal Resistance of Ultrafast Sub-micron InP/InGaAs SHBTs

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Abstract

This work reports experimental data for the thermal resistance and junction temperature of high-performance InP/InGaAs single heterojunction bipolar transistors (SHBTs). The effects of device scaling and layer epitaxial design are investigated, and a theoretical model is developed to examine the results.

INTRODUCTION

Recently, high-speed InP/InGaAs HBTs have been reported to achieve cutoff frequencies in excess of 500 GHz [1]. These devices operate at current densities above 1000 kA/cm^2, and thus generate considerable interest in determining the device operating temperature for reliability concerns. This work presents thermal resistance and junction temperature for ultrahigh-speed InP-based single heterojunction bipolar transistors, with experimental data showing scaling effects of device length and epitaxial structure.

LAYER STRUCTURE

The thermal resistance and junction temperature of two epitaxial structures are compared in this work. Both wafers are MBE grown on Fe-doped semi-insulating InP substrates. The first epitaxial structure, denoted as UIUC150, consists of a 150 nm InGaAs collector and 30 nm graded base C-doped at 5 x 10^{19} cm^{-3}. This structure exhibits peak RF performance of f_T = 382 GHz on a 0.5 × 12 μm^2 device [2]. The second structure, UIUC75, is similar to the first, with the exception of a 75 nm InGaAs collector and a 25 nm base doped at 6 x 10^{19} cm^{-3}. This structure exhibits typical f_T values of 485 GHz for 0.5 μm emitter width devices [1].

RESULTS

Thermal resistance and junction temperature were acquired for the two substrates detailed above using a multiple substrate temperature technique consisting of two sets of I-V measurements [3, 4]. The first measurement forces a constant V_{CE} while sweeping I_B for multiple V_{CE} values, with the chuck held at room temperature. The second measurement forces a constant V_{CE} taken at substrate temperatures between 25 °C and 75 °C, and is used as calibration data when overlaid with the first set of measurements. By evaluating multiple intersection points of the overlaid curves at a fixed collector current, a system of equations can be solved to yield R_{TH} and T_j. This technique is illustrated in Fig. 1, where the black lines correspond to the first set of measurements, and the gray lines to the calibration data acquired at multiple chuck temperatures.

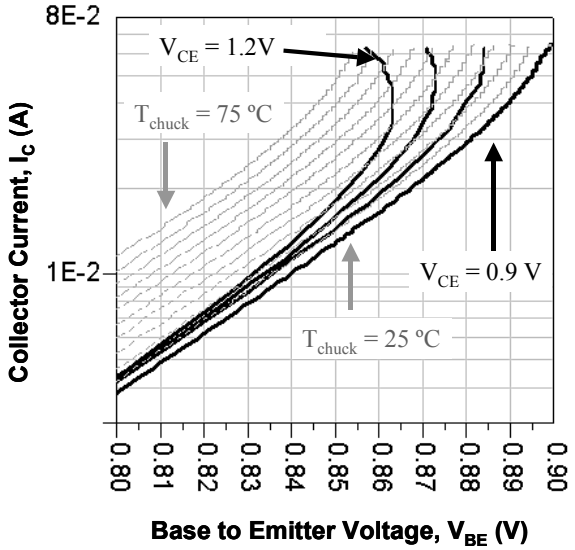

Fig. 1. Example thermal resistance measurement. Black lines represent room temperature measurements with V_{CE} fixed at values between 0.9 V and 1.2 V. The gray lines represent V_{CE} = 0.9 V curves at chuck temperatures ranging from 25 to 75 °C.

Fig. 2 shows junction temperature, T_j, and f_T versus collector current density, J_C, for 0.5 x 8 μm^2 transistors fabricated on both epitaxial structures. At the peak f_T current density, UIUC150 has a junction temperature of 101 °C at 560 kA/cm^2, corresponding to an f_T of 366 GHz. The UIUC75 device has a junction temperature of 98 °C and an f_T of 430 GHz at the same current density. Due to the thinner collector in the UIUC75 structure, the peak performance (f_T = 480 GHz) occurs at a much higher current

density of Jc = 1100 kA/cm^2, corresponding to a T_j of 175 °C. The junction temperature of the devices is found to be linearly proportional to current density, as shown in Fig. 2.

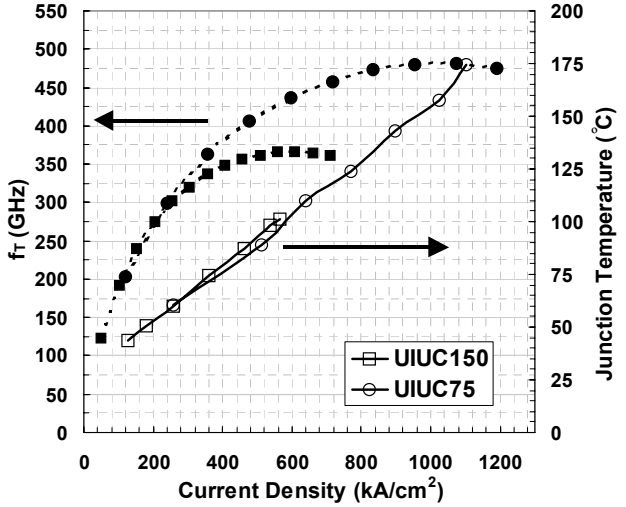

Fig. 2. f_T and T_j vs. J_C for collector thicknesses of 150 nm (squares) and 75 nm (circles) on 0.5 × 8 μm^2 SHBTs.

The thermal resistance, normalized to junction area, and junction temperature are plotted versus current density in Fig. 3 for HBTs with emitter lengths of 3, 8, and 12 μm (W_E = 0.5 μm). For a fixed current density, T_j decreases for devices with smaller active area at a fixed current density as expected. It is important to note that the thermal resistance of the UIUC75 device is very slightly less than UIUC150. This subtle difference is attributed to an overall thinner layer of InGaAs in the epitaxial stack; the UIUC150 structure contains 580 nm of InGaAs in the base, collector, and subcollector layers, while UIUC75 contains a total of only 400 nm of InGaAs. The current density and junction temperature at peak RF performance for devices from the UIUC75 structure are 1190 kA/cm^2 and 153 °C for a 0.5 x 3 μm^2 device, 1100 kA/cm^2 and 175 °C for a 0.5 x 8 μm^2 device, and 1000 kA/cm^2 and 165 °C for a 0.5 x 12 μm^2 transistor. The results are summarized in Table I, including the RF performance of each device when operating at T_j = 125 °C, an important figure of merit for maintaining adequate device lifetimes and good reliability.

ANALYSIS

Various thermal modeling studies of double heterojunction bipolar transistors (DHBTs) have shown that the dominant thermal conduction path is down through the collector and subcollector layers, spreading into and through the InP substrate [5]. While the thermal resistance values for DHBT devices are comfortably low, a SHBT device structure in which the thermal conductivity of the InGaAs collector and subcollector layers is an order of magnitude lower would seem to result in a catastrophically high thermal resistance value. This in turn would lead to excessive junction temperatures and severe reliability problems at current densities of interest for high performance applications. However, the SHBT measurements above exhibit reasonable junction temperatures (T_J=125 °C at 808 kA/cm^2 and T_J=175 °C at 950 kA/cm^2) and acceptable thermal resistance values at very high current densities.

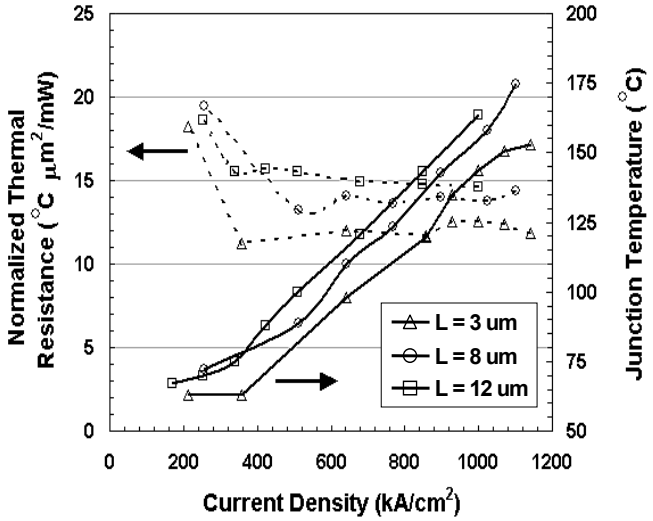

Fig. 3. Normalized RTH and Tj for UIUC75 SHBTs with lengths of 3 μm, 8 μm, and 12 μm. WE = 0.5 □m for all devices.

TABLE I

Measured thermal resistance, junction temperature, and RF performance for UIUC75 transistors with W_E = 0.5 μm and lengths of 3, 8, and 12 μm.

	@ Peak Current Density				@ T_j = 125 °C		
	R_{TH} (°C/mW)	T_j (°C)	f_T (GHz)	f_{MAX} (GHz)	J_C (kA/cm^2)	f_T (GHz)	f_{MAX} (GHz)
0.5 x 3 μm^2	8.438	152.7	473	288	895	460	290
0.5 x 8 μm^2	3.698	174.6	481	231	808	470	241
0.5 x 12 μm^2	2.481	163.5	470	201	728	428	203

The thermal resistance values are calculated for the collector, θ_C, and subcollector, θ_{SC}, layers of the 3 μm, 8 μm, and 12 μm (W_E = 0.5 μm) devices on the UIUC75 epitaxial structure. The current spreading between the emitter and collector is assumed to increase the effective stripe width from 0.5 μm to 0.6 μm, and the effective width of the thermal path through the subcollector exceeds the effective width through the collector layer by an amount equal to the thickness of the subcollector layer. The result of this simple calculation of SHBT collector and subcollector thermal resistances is shown, along with their sum, θ_{C+SC}, and that sum normalized to the emitter area, $A_E\theta_{C+SC}$, in Table II. Note that on an area-normalized basis, the SHBT gives $A_E\theta_{C+SC}$ = 37 °C μm^2/mW for a 0.5 × 8 μm^2 SHBT. These numbers for just the collector+subcollector component of the thermal resistance exceed the total junction to "case" (substrate wafer backside or chuck) thermal resistance values measured by a large factor of 3 to 4.

The discrepancy between the calculations made above and the actual measured data can be explained by the fact that the simple model used for the calculations in Table II fails to consider that when a thermal conductivity value is degraded by a factor of 10, the result cause a completely different thermal path, one that may have been insignificant originally, to become the dominant conduction path. The alternate thermal path for a SHBT is through the emitter contact into the interconnect metallization rather than down through the poorly conductive InGaAs collector and subcollector layers. Furthermore, the UIUC interconnect scheme and RF overlay pad design are ideally suited for thermal dissipation through the pad metallization. The etchback procedure used to expose the emitter contact directly to the 1 μm gold metallization layer inherently incorporates a top-side thermal shunt path for the device. The overlay metal covers the length of the emitter metal strip, providing a large thermal sink in the form of the emitter ground pad.

TABLE II

Thermal resistance values obtained for a standard collector/subcollector thermal conduction path model, along with normalized measured results for a 75 nm collector epitaxial structure.

	Substrate Model				Measured
	θ_C (°C/mW)	θ_{SC} (°C/mW)	θ_{C+SC} (°C/mW)	$A_E\theta_{C+SC}$ (°C-μm²/mW)	$A_E\theta_{JCase}$ (°C-μm²/mW)
0.5 x 3 μm²	6.72	16.34	23.06	34.59	12
0.5 x 8 μm²	2.572	6.614	9.186	36.74	13.8
0.5 x 12 μm²	1.722	4.48	6.20	37.21	15.2

Figure 4 illustrates a model for a SHBT with an emitter thermal shunt path to the semi-insulating InP substrate, along with its simple thermal model at the right. A contact stripe (subcollector or gold) to backside thermal spreading resistance of 1.9 °C/mW was assumed for an 8 μm long stripe. Table III shows the results obtained from modified calculations including the emitter thermal shunt shown in the SHBT layout and thermal model in Fig. 4, as applied to the same devices of Table II. The first column of entries for the collector/subcollector path is the same as the third column of Table II, except for the addition of the substrate thermal spreading resistance. The second column gives the thermal resistance through the emitter and metallization path. The third column in Table III gives the total junction to case thermal resistance values, θ_{JCase}, for the SHBTs, obtained as the parallel combination of the first two columns.

TABLE III

Thermal resistance values obtained for a modified emitter thermal shunt path, including thermal resistance values for the collector-side shunt (C+SC), emitter shunt (ES), and parallel combination of the two (Parallel).

	Substrate Model				Measured
	θ_{C+SC} (°C/mW)	θ_{ES} (°C/mW)	θ_{JCase} (Parallel) (°C/mW)	$A_E\theta_{JCase}$ (°C-μm²/mW)	$A_E\theta_{JCase}$ (°C-μm²/mW)
0. 5 x 3 μm²	23.8	7.37	5.63	22.5	12
0.5 x 8 μm²	11.1	5.5	3.68	14.7	13.8
0.5 x 12 μm²	9.05	5.84	3.55	14.2	15.2

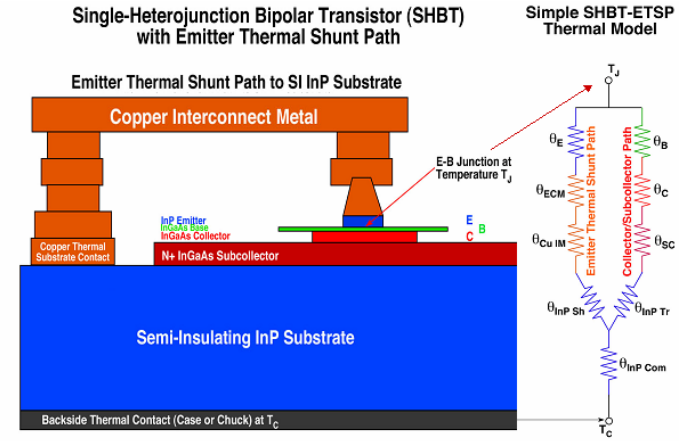

Fig. 4. Equivalent circuit and schematic cross section for emitter thermal shunt model.

The thermal resistance calculations utilizing the emitter shunt path agree very well with the experimentally measured values. The thermal resistance values could be lowered further by increasing the gold overlay metallization thickness, and by additional engineering of both the emitter and collector/subcollector epitaxial structure [5]. Modifying the emitter cap layer by reducing the InGaAs thickness or grading the cap to a strained InAs layer would enhance the overall thermal conductivity of the emitter. Also, by replacing the bulk of the subcollector with InP, which can be accomplished by constructing a subcollector primarily of heavily-doped InP with a thin InGaAs layer to allow ohmic contacts, the thermal resistance can be dramatically reduced. For aggressively scaled epitaxial structures in which the InGaAs thickness in the collector and subcollector is minimal, the total thermal resistance of SHBT devices will approach that of DHBTs.

Even without these additional improvements, the measured θ_{JCase} values show that SHBT devices are acceptable for high-performance, high current density applications while maintaining reasonable junction temperatures. It is critical to mention, however, that the devices used in the construction of such high-speed circuits must contain some form of emitter thermal shunt, whether it be from an individual shunt path to the substrate for each "hot" device, or from interconnect metal which provides an adequate thermal sink, to allow the devices to conduct heat

effectively through the emitter; the lack of a conductive thermal path through the emitter will result in thermal resistance values similar to the calculated values in Table II and ultimately lead to catastrophic failure of the circuit.

A final point worth noting is that the measurement technique described above gives the temperature at the emitter-base (E-B) junction. The authors estimate that the temperature in the InGaAs collector layer would be higher than that at the E-B junction, and these θ_{JCase} values do not actually define the highest temperatures in the SHBT device. On the other hand, most of the deterioration criteria (e.g., ΔV_{BE} and $\Delta\beta$) used in reliability studies tend to be associated with the base or the E-B junction regions, and therefore it is irrelevant whether the collector junction operates at a slightly higher temperature than the E-B junction.

CONCLUSION

The junction temperature and thermal resistance of high-performance SHBTs have been investigated. The measured results show that the thermal catastrophe expected for high current density single heterojunction devices is averted due to an alternative thermal conductive path through the emitter of the device, as long as a thermal path is provided from the emitter of the device to the substrate. Calculations performed including this conductive path show good agreement with measured results. These findings indicate that SHBT devices can be reliably implemented in high-speed applications requiring high current densities.

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REFERENCES

[1] W. Hafez, J.-W. Lai, and M. Feng, "InP/InGaAs SHBTs with 75 nm collector and f_T > 500 GHz," *IEE Electronics Letters*, vol. 39, pp. 1475-1476, 2003.

[2] W. Hafez, J. W. Lai, and M. Feng, "Record f_T and $f_T + f_{MAX}$ Performance of InP/InGaAs Single Heterojunction Bipolar Transistors," *IEE Electronics Letters*, vol. 39, pp. 811-813, 2003.

[3] W. Liu and A. Yuksel, "Measurement of junction temperature of an AlGaAs/GaAs heterojunction bipolar transistor operating at large power densities," Electron Devices, IEEE Transactions on, vol. 42, pp. 358-360, 1995.

[4] W. Liu, H.-F. Chau, and E. Beam, III, "Thermal properties and thermal instabilities of InP-based heterojunction bipolar transistors," Electron Devices, IEEE Transactions on, vol. 43, pp. 388-395, 1996.

[5] S. Thomas, III, J. A. Foschaar, C. H. Fields, M. M. Madhav, M. Sokolich, R. D. Rajavel, and B. Shi, "Effects of device design on InP-based HBT thermal resistance," Device and Materials Reliability, IEEE Transactions on, vol. 1, pp. 185-189, 2001.

ACRONYMS

HBT: Heterojunction Bipolar Transistor
MBE: Molecular Beam Epitaxy
SHBT: Single Heterojunction Bipolar Transistor
DHBT: Double Heterojunction Bipolar Transistor
RF: Radio Frequency