Walkout in PHEMTs: Origin and Relation to Device Structure

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Abstract

Parameter walkout of more than 250 power $Al_{0.24}Ga_{0.76}As/In_{0.25}Ga_{0.75}As/GaAs$ double-recessed PHEMTs with different layout geometry and epitaxial structure has been experimentally measured and simulated. The relation between DC, small-signal and large-signal behavior has been recognized. The essential parameters of walkout were defined; their geometry and structural dependence have been derived. Possible methods of walkout control are discussed.

INTRODUCTION

The AlGaAs/InGaAs/GaAs pseudomorphic high electron mobility transistors (PHEMTs) are used for a number of high frequency applications. Power applications of electronic components at high frequencies require very stable performance. Therefore, any changes in the DC and RF parameters of a device during normal operation conditions, i.e., performance walkout, make the device unacceptable for these applications. To eliminate the causes of walkout in PHEMTs it is vital to determine its mechanisms.

The performance walkout, i.e., the anomalous increase in the drain current (I_D) at high drain-source voltages (V_{DS}) is a damaging phenomenon often observed in HEMTs and AlGaAs/GaAs HFETs [1-3]. It results in transconductance suppression (Δg_m^{max}), shifts in threshold voltage (ΔV_T) and consequently in deviation from the optimal load line for these transistors. Although many papers have been dedicated to the walkout, its physical origin and the ways to eliminate it are still debated [2-3].

The aims of this research are a) to determine the physical origin of walkout and b) to reveal the correlation between PHEMT walkout and its physical structure and geometry. The walkout could be parameterized in terms of a permanent shift of the main PHEMT figures of merit: threshold voltage (ΔV_T), maximum transconductance value (Δg_{mmax}), small-signal maximum available gain (ΔMAG), and threshold frequency (Δf_T).

EXPERIMENTAL

Since the original work of Menozzi et al. [1], the role of impact ionization as the walkout-triggering phenomenon for GaAs-based heterostructure transistors has been shown by several workers [2-3]. Hot holes, created by impact ionization, are either captured by hole traps or compensate trapped electrons, thus making the net charge in the region between source and drain more positive. Therefore, there is a need to apply a more negative gate-source bias (V_{GS}) to close the transistor channel – i.e., the threshold voltage shifts to negative values. Hence, the threshold voltage shift (ΔV_T) is our first convenient figure of merit for walkout characterization.

Table 1 Layout dimensions of the Device Zoo

L_{DS}[μm]	L_{SG}[μm]	L_{SR}[μm]	L_G[μm]	L_R[μm]
2 ÷ 4	1.2 ÷ 1.6	0.8 ÷1.1	0.15÷0.3	1 ÷1.7

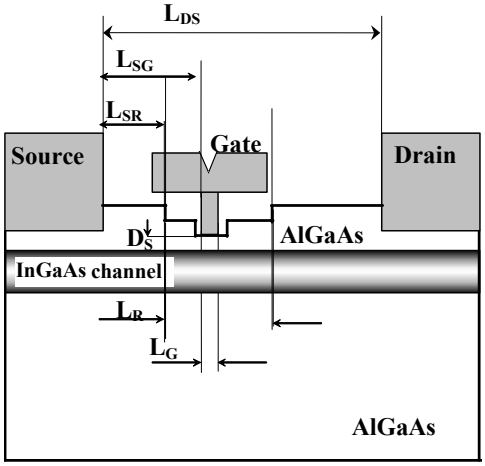


Figure 1 Schematic diagram of the double-recessed PHEMT. The source-drain distance (L_{ds}), source-gate distance (L_{sg}), source-recess distance (L_{sr}), recess width (W_r), and gate length (L_g) are layout parameters changed in the experiment are indicated. Their numerical values are given in Table I. Distance from the gate foot to the channel – D_s is the Schottky layer thickness.

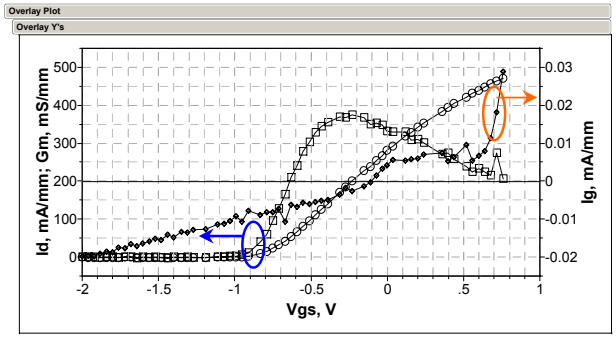
A 0.25 μm gate double recessed power PHEMT was used as the basic element for this research. Figure 1a shows a typical cross-section of such a PHEMT indicating the key geometrical layout parameters. They are: L_{ds}-source-drain distance, L_{sg}-source-gate distance, L_{sr}-source-recess distance, L_r-recess width and L_g-gate length. The second (gate) recess is factually defined by the gate length, as shown in figure 1. Its width is slightly wider than the gate foot and its depth determines the Schottky layer thickness. The process details are published elsewhere [4]. Since the lateral geometrical parameters and their interactions have a complex effect on impact

ionization, the Device Zoo approach has been used [4]. Measurements of more than 250 PHEMTs, differing by both lateral and vertical geometries, have been performed. An empirical model, relating walkout parameters and device structure, has been developed.

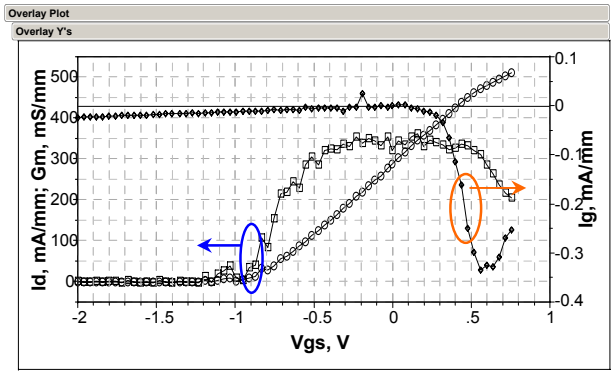
All measurements used a HP 4551B semiconductor analyzer, vector network analyzer HP 8510C and RF probes. The statistical analysis of the data was carried out using SAS software (JMP 5.0). The Silvaco Fast Blaze Mercury software was used for simulation of the electric field in the PHEMT and estimation of the trapped charge effect.

RESULTS AND DISCUSSION

A. Empirical models



a)



b)

Figure 2 a) Typical performance of a PHEMT, measured at Vds = 2 V; b) Typical performance of the same PHEMT measured at Vds =7V.

Typical I-V characteristics, i.e., I_D and I_G as a function of V_{GS}, for the PHEMT in question are shown in figure 2a, solid line, V_{DS} was held during the measurements at 2 V. Figure 2b shows the electrical characteristics of the same device at a higher V_{DS} = 7 V. The typical pattern of impact ionization could be seen at the gate current vs. gate-source bias V_{GS} curve in the V_{GS}= 0 ÷ 0.5 V region – the region of the gate current peak [5-7]. The dashed line in figure 2a presents the I-V curve of the same device after the measurement at V_D = 7 V, measured at V_D = 2 V. The V_T shift is about 0.2 V to the more negative bias.

The energy bands of the PHEMT are shown in figure 3, where energy and the distance from the semiconductor surface are the vertical and horizontal axes, respectively. We hypothesize the presence of acceptor-like

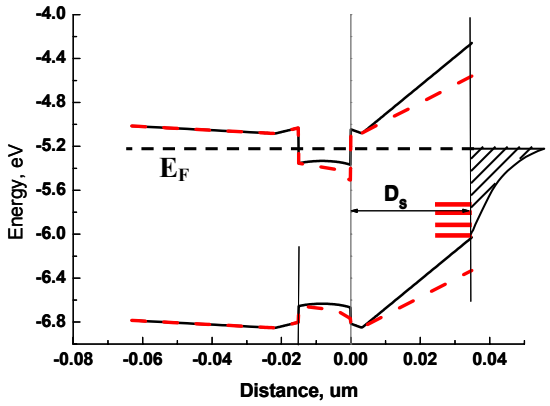


Figure 3. Schematic view of the PHEMT energy bands dependence on distance from the gate. The dashed curve presents

states at the surface of the intentionally undoped $Al_{0.23}Ga_{0.77}As$ Schottky layer that are negatively charged in the initial state. The hot holes generated during impact ionization have enough energy to surmount the 0.2 eV of the energy barrier and drift through the Schottky layer to the surface, while hot electrons are confined by the internal electric fields. Holes are trapped by the acceptor-like states and compensate the negative charge. As a result the energy bands shift from the initial position and the RF and DC characteristics of the PHEMT are changed.

To check the hypothesis, devices have been submitted to electrical stress at different constant V_{DS}, while the V_{GS} was ramped up in three different regions: Region1) Outside the impact ionization region, negative gate current, $V_{GS} \in [-2, -0.3]$ V; Region 2) Outside the impact ionization region, positive gate current, $V_{GS} \in [0.6, 0.65]$ V; Region 3) Within the -impact ionization region, $V_{GS} \in [0.2, 0.6]$ V. We will refer to this type of stress as the impact ionization stress. The V_{DS} bias varied for each type of stress from 5 V to 17 V with 1 V steps.

To monitor the walkout level, DC and small-signal RF measurements were performed at V_{DS} = 2 V before and after of step of the V_{DS} ramping. Biasing at negative gate currents (region 1) does not change the device performance up to V_{DS} = 17 V. Biasing in region 2 results in tiny changes in the DC and RF performance (less than 1% of the initial value) while biasing within region 3 results in a major change of both DC and RF parameters. Therefore, the hot hole stress leads to the observed walkout. Figure 4 shows the I_D and I_G as a function of the V_{GS} before and after impact ionization stress. The change in I_D results in V_T changing from -0.92 V to -1.16 V, while I_G does not change.

Thus, the following discussion of electrical stress is limited to region 3. To model the walkout effect, the impact ionization stress was applied to a Device Zoo matrix. Figure 5 shows the threshold voltage (V_T) as a function of the applied V_{DS} for the Device Zoo matrix.

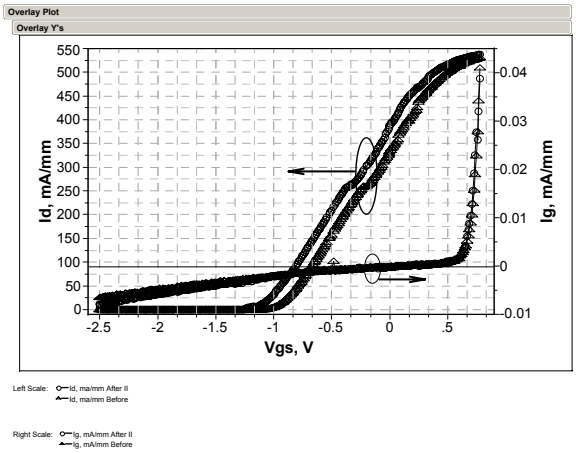


Figure 4. I_G and I_D as a function of V_{GS} before and after impact ionization stress. The triangles relate to the I-V characteristics before impact ionization

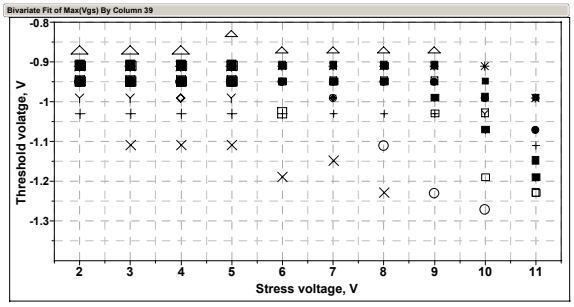


Figure 5. The threshold voltage for 16 devices of the Device Zoo as a function of the stress voltage applied at drain-source.

V_T values for 16 PHEMTs, varied by layout parameters, are plotted for each V_{DS} value. Since the devices within the Device Zoo vary by layout parameters, an empirical model for the V_T dependence on layout parameters could be created. The spread of the V_T values exists both for the initial and the stressed states and V_T for each transistor decreases with increasing V_{DS}, differently for each device. A stepwise regression fitting has been performed to reveal the empirical relation between V_T and PHEMT layout parameters. Details of the modeling could be found elsewhere [5].

The empirical model (equation 1), developed for the initial distribution of V_T shows that the gate length (L_G) is the sole layout parameter affecting V_T – as shown in figure 6a - which agrees with theory [6].

$$V_T = -1.03 + 0.4 * L_G \qquad 1$$

The smaller the gate length and consequently the width of the gate recess, the higher is the negative potential that should be applied to the gate to close the PHEMT channel.

The empirical model for the distribution of V_T after stress at V_{DS} = 11 V shows that the relationship between V_T and the layout parameters changes from the initial state: the recess width L_R becomes the key parameter with the same dependence as L_G before the walkout. The recess position also influences V_T, represented by the coefficient L_{SR}. Equation 2 presents the coefficients for the V_T distribution of the PHEMTs after walkout.

$$V_T = -2.06 + 0.55 * L_G + 0.3 * L_{SR} + 0.34 * L_R \qquad 2$$

The dependence of V_T on L_G, L_R and L_{SR} is presented in figure 6b. The wider the first recess, the less negative potential has to be applied to the gate to close the channel. This analysis leads us to conclude that the recess surface area works as an effective gate, sharing in the charge control of the channel. Therefore, the parasitic charge is captured within the recess area only. The gate diode measurements show that the diode characteristics: the Schottky barrier height (V_B) and the ideality factor (n) have changed by less than 5 % from the initial value, which is negligible in comparison with the 0.3 V V_T shift..

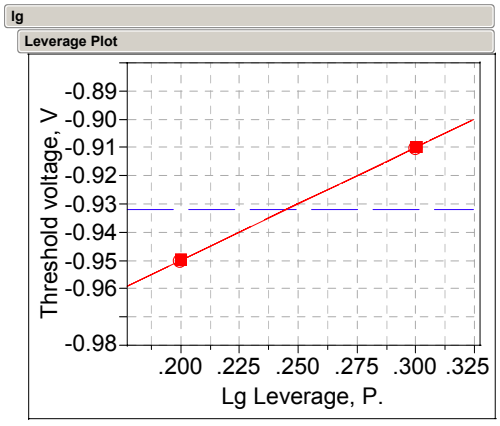


Figure 6a. V_T as a function of the gate length within the matrix before stress. The lines of 95% confidence coincide with the fitted line; dashed line presents the mean value.

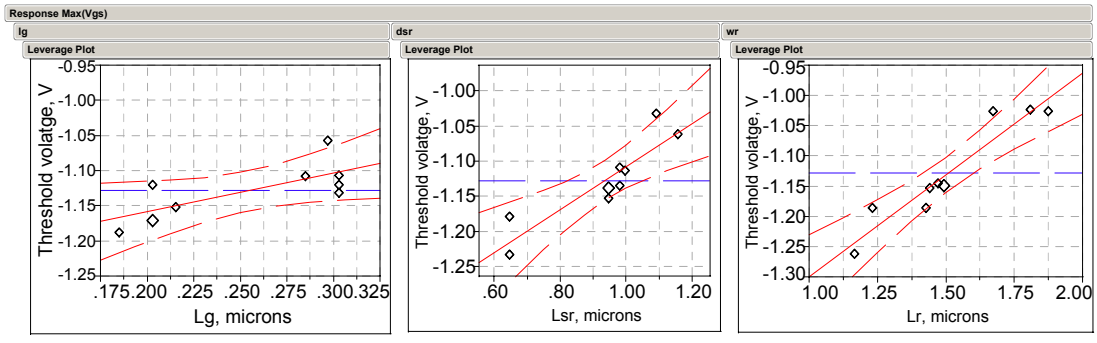


Figure 6b. V_T within the matrix after impact ionization stress at 10 V, as functions of L_G, . L_{SR}, L_R. Red line is the function fitted to the experimental points. Dashed lines present the mean values. Long-dashed red lines are lines of 95% confidence in fitted line.

Therefore, we can exclude the gate foot/AlGaAs interface a possible location where the charge is captured. Hence, the parasitic charge is localized between the gate and the recess walls and, according to the model, is directly proportional to the recess width - L_R. The physical explanation of the dependence on the recess position, i.e., to L_{SR}, involves impact ionization. It is L_{SR}, which affects the electric field value within the channel, because at constant L_R and L_G, L_{SR} determines the distance between the gate and the n-doped GaAs cap layer on the drain side. The closer is the gate position to the drain side of the recess, i.e., the smaller is L_{SR}, the higher are the impact ionization rate and the hot hole concentration. Increasing the hot hole concentration results in higher probability of their trapping and in higher V_T negative shifts. Therefore the walkout is governed by overlap of two effects – the high electric field between gate and drain, determined at the PHEMT layout level by L_{SR} and the available space for surface traps, related at the PHEMT layout level to L_R.

Since the target applications of PHEMTs are high frequency ones, any changes in the RF performance are critical. The main PHEMT RF figures of merit for the circuit design are the maximum available gain (MAG, measured in dB), and the unity current gain frequency (f_T) [7]. An analysis of the changes in the MAG and f_T has been performed on the same Device Zoo matrix as for the DC performance. The change of the f_T can reach 12 GHz, depending on the layout. In agreement with our work hypotheses, the accumulated charge near the gate leads to decreasing of the depletion area width. It results in increasing the gate-channel capacitance and in decreasing of f_T, which is consistent with theory [7]. Therefore, f_T, chosen as a RF modeled parameter, could provide physical insight to the structural origin of the walkout. The f_T values have been parameterized and modeled by the same method that was described for the threshold voltage. Equations 3 and 4 present the empirical dependencies for f_T at the initial state, and after stress at V_D = 11 V, respectively.

$$\mathbf{f_T = 38.12 - 54.47*L_G - 5.52*L_R} \qquad \mathbf{3}$$

$$\mathbf{f_T = 35.55 - 39.69*L_G - 8.87*L_R} \qquad \mathbf{4}$$

The two equations above express the same physical meaning of the equations for V_T – the contribution of L_G decreases and the impact of L_R is much stronger after stress. L_R is present in both equations 3 and 4 for f_T because f_T is highly dependent on the input gate-source capacitance, which is related to the recess width. However, L_R has a larger coefficient in the post-stress case and thus plays a more dominant role than L_G. The two models, for V_T and for f_T are in good agreement.

Thus, walkout impact on device performance is closely related to the L_R and L_{SR}, i.e. to the recess surface area.

B. Possible Solutions

It is possible to tune the walkout phenomenon by layout parameters only: the impact ionization rate by gate and recess position, and the area exposed for hole capture by the recess width. However, the price for the recess width decrease is the reduction of the breakdown voltage and the recess cannot be reduced up to infinitely small value. Nevertheless, it is the electric field that governs the transistor performance, and the electric field is essentially two-dimensional. Therefore, the vertical structure could be modified in such a way that the impact ionization generated holes cannot reach the surface. The idea is to change the vertical epi-structure in such a way that the internal electric field impedes the hot hole capture at the recess surface.

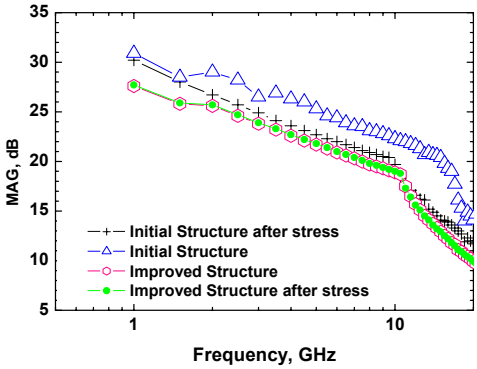


Figure 7 MAG as a function of frequency for two PHEMTs with identical layout and different vertical structure before and after stress.

PHEMTs with improved vertical structure have been manufactured and measured. The analysis shows that ΔV_T decreases from 0.24 V to 0.05 V under the same conditions and ΔMAG from 2.3 dB to 0.03 dB. Figure 7 shows the dependence of MAG for two PHEMTs with the same layout and different vertical structures before and after walkout. The MAG for the PHEMT, manufactured on the improved structure, changes by less than 2% after walkout.

III. CONCLUSION

Walkout impact on device performance is closely related to the recess surface area. Empirical models for the correlation between device layout and walkout parameters have been developed. The design of epi-structure makes it possible to avoid walkout of PHEMT.

IV. ACKNOWLEDGMENTS

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