Sub-Surface Damage Removal in Fabrication & Polishing of Silicon Carbide

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Abstract

Silicon Carbide (SiC) is emerging as a promising substrate for systems which leverage the low lattice mismatch with Gallium Nitride (GaN), high power density, heat dissipation and radiation hardness properties unique to this semiconductor. Wafer fabrication and polishing of SiC substrates poses processing issues as a result of the material's high Mohs hardness (~9.25), and chemical inertness. Particularly important to epitaxial layer nucleation on these wafer surfaces is an atomically smooth finish free of sub-surface damage, which is invisible to most inspection methods. Prime damage-free surfaces will ideally exhibit bi-layer terraces corresponding to plane (0001) edges. II-VI has achieved such damage-free surfaces by closely monitoring damage through molten KOH etching and optical characterization, and developing a chemo-mechanical polish (CMP) process that effectively reveals this damage while simultaneously removing it.

Origin and Characterization of Sub-Surface Damage After Mechanical Polishing

Mechanical polishing of SiC is typically done with diamond based slurries, where the abrasive size is successively reduced and eventually ending with a sub-micron slurry to achieve the desired roughness. Surfaces with low average roughness (Ra < 5Å) can be achieved (see Figure 1) relatively easily. These surfaces can be featureless or show some minimal polishing damage under AFM microscopy. However, after high-temperature thermal processing prior to or during epitaxial growth, a dense network of scratches and defects can be revealed. This network corresponds to the sub-surface damage or dislocation network impacted into the SiC surface during the mechanical abrasion process. Figure 2 shows an optical microscope picture of a thermally treated surface, which previously exhibited roughness typical of Figure 1 before thermal etching. Scratch depth invisible to the eye can be revealed to be as high as 150Å. However, this damage can be revealed *in-situ* during either metal organic chemical

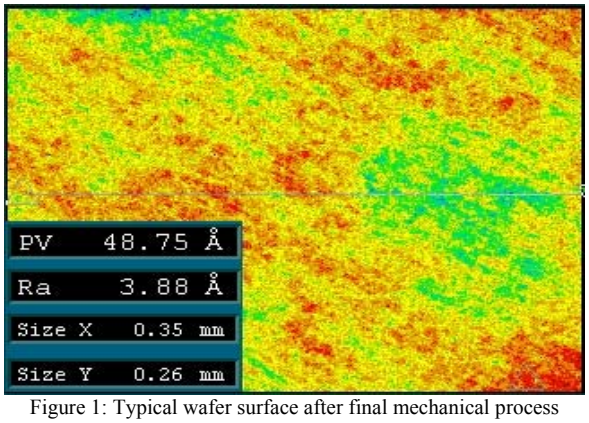

Figure 1: Typical wafer surface after final mechanical process (Zygo® normal white light interferometry)

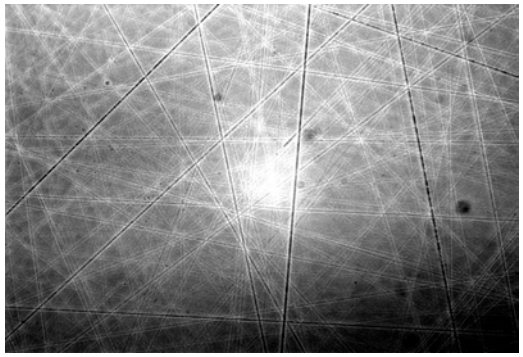

Figure 2: Thermal Revelation of Sub-Surface Damage (350 x 260µm) at ~1600°C.

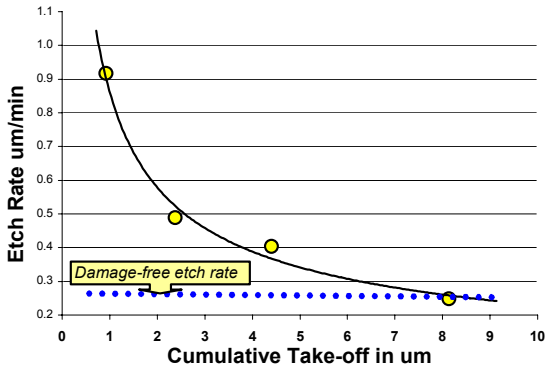

Figure 3: Etch Rate in KOH @450°C of a mechanically polished SiC wafer as a function of material removed showing reduction in etch rate with time.

vapor deposition (MOCVD) growth during an initial hydrogen purge at high temperature, or more drastically during molecular beam epitaxy (MBE) by 3-dimensional preferential growth around such defects.

As with other semiconductors, this sub-surface damage can easily be revealed by selective etching. However in the absence of a room temperature selective etch for SiC, molten salt etching is often employed. II-VI has made use of a previously established molten KOH etching [1] technique to expose and characterize this sub-surface damage. In our case, etching is carried out at 450°C within a nickel crucible inside a vertical ceramic furnace. As is evident in the example of Figure 3, the etch rate is much higher in the damaged surface region and reduces quickly, approaching an asymptotic rate (shown as dotted horizontal line in figure) as the damage is removed after a few microns.

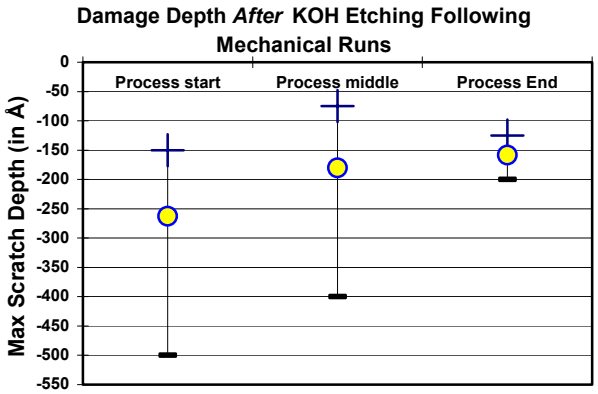

Figure 4: Maximum mechanical sub-surface damage depths

Using this etch technique, the depth of damage can easily be assessed at every stage in the process. Damage can thereby be reduced to a minimum by careful attention to the normal array of polishing process parameters available (slurry types, sizes, proper distributions, pressures, rotation rates etc). Minimization of sub-surface damage after the final stage of the mechanical polishing process to <150Å is routinely achieved (see Figure 4).

SUB-SURFACE DAMAGE REMOVAL IN SIC

Chemical-mechanical polishing is often the last and most critical step in the polishing process of many semiconductors such as Si and GaAs. In these materials the process utilizes the combination of a chemical oxidation reaction followed by mechanical abrasion or secondary chemical reaction. The continuous and simultaneous friction and chemical attack leads to material removal resulting in extremely planar surfaces with zero or near zero sub-surface damage, as the abrasive can be of significantly lower hardness than the non-affected substrate material. Unfortunately in the case of SiC, its combined chemical inertness and hardness leads to very low removal rates during conventional CMP techniques such that sub-surface damage cannot be removed in a timely manner. Additionally, a directly proportional relationship has been indicated with respect to wafer surface orientation. As surfaces approach a perfectly planar (0001) or "c" plane, process time increases appreciably, as fewer planar edges

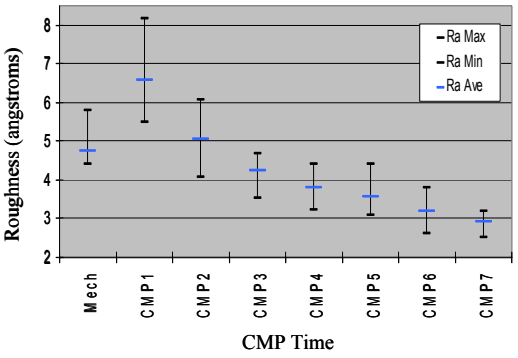

Figure 5: Surface evolution during CMP

are available for reaction. II-VI has developed a modified CMP process to fully eliminate sub-surface damage, and resulting stress in an acceptable process time.

Figure 5 shows an example of the roughness evolution of a typical surface at various interrupted test points during the CMP process (designated CMP1, 2 etc.) and demonstrates the capacity of the technique for planarization and damage removal. The roughness in this case is measured with white light interferometry and each point represents an average of 5 points on each of multiple wafers within a polish run. The first data point represents the average run roughness as received from the last mechanical step in the process (in this case Ra ~4.5A). Shortly after the start of CMP the roughness actually

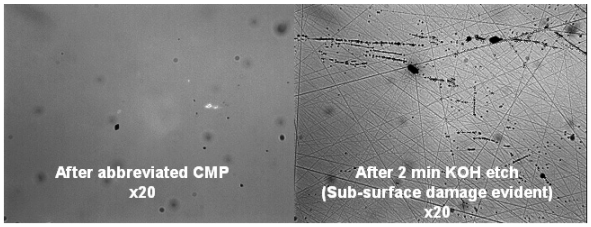

Figure 6a: Surface following abbreviated CMP before and after molten KOH etching revealing sub-surface scratches.

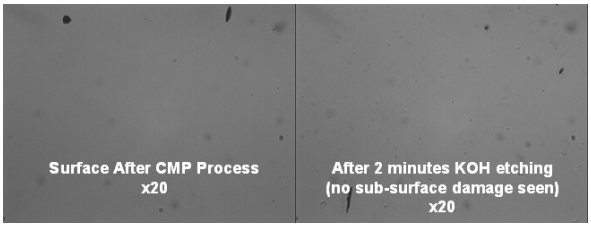

Figure 6b: Surface after full CMP before and after etching (no scratches evident).

increases as the dislocated, damaged sub-surface material is revealed and removed, exposing scratch trenches and abrasion pits. After a further period the roughness begins to reduce as the CMP continues to planarize the wafer face, approaching an even, common atomic plane across the wafer surface. Finally, as the process proceeds, the average roughness falls below the starting value and is brought below 3 angstroms in a timely manner. Notice also that the range of the roughness values within the run tighten up considerably. Clearly, planarization and damage removal is occurring. Damage removal is unambiguously confirmed after molten KOH etching where no sub-surface damage features are revealed beyond threading dislocations (Figure 6).

Characteristics Of Production Wafers

Figures 7, 8, and 9 show final Ra, Ra Range, and PV (peak-to-valley) roughness values on a 350 x 260 field of view as measured by a Zygo ® New View 5010 optical interferometer. 95.8% of wafers sold exhibited final Ra below 2.5Å. As the process ends in an atomically smooth

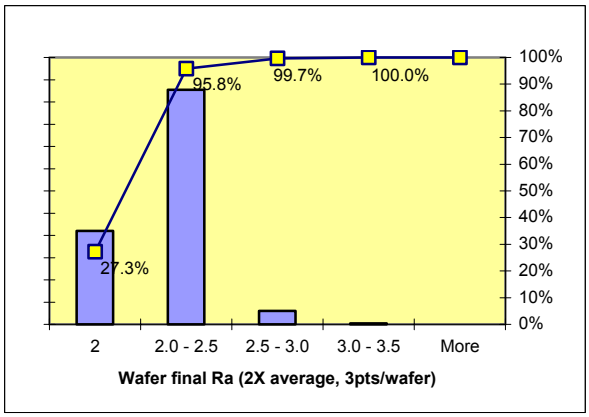

Figure 7: Final Ra Values for Wafers Sold to Date

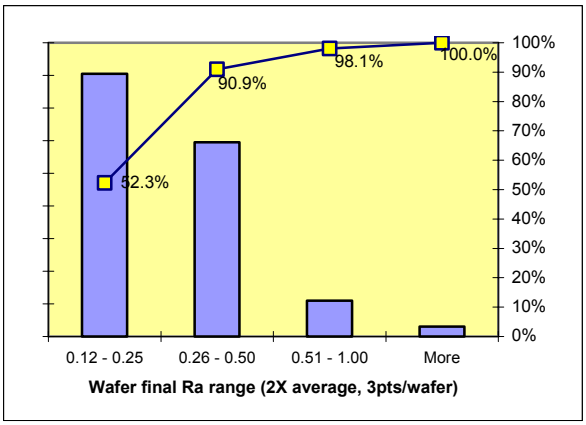

Figure 8: Final Ra Range for Wafers Sold to Date

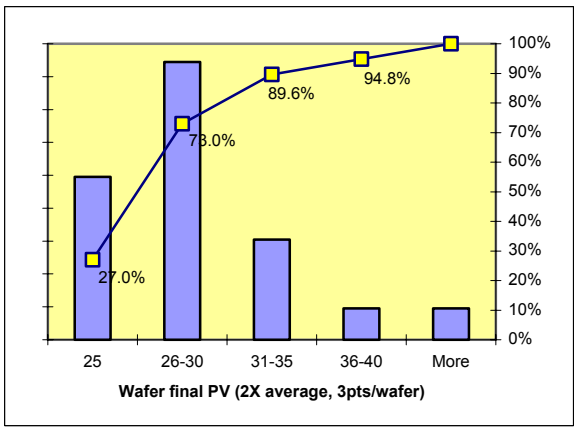

Figure 9: Final PV for wafers Sold to Date

surface, it allows for not only very smooth and planar surfaces, but also very consistent results. 90.9% of wafers showed a range in Ra of within 0.5 Å, and 52.3% within 0.25Å. Results at these fields of view correspond to 5µm x 5µm AFM scans of consistently below 1Å with clear atomic terracing visible (see Figure 10 below). As seen in figure 9, PV (peak-to-valley height) on 89.6% of II-VI wafers averaged below 35Å (3.5 nm), and 27.0% lower than 25Å (2.5 nm). PV on most commercially available surfaces average from 4 to 12 nm (40 to 120Å)

Customer Validation Via Atomic Force Microscopy (AFM)

Wafers have been sold to and successfully validated by government and commercial customers. For all customers, successful hetero- and/or homo-epitaxial

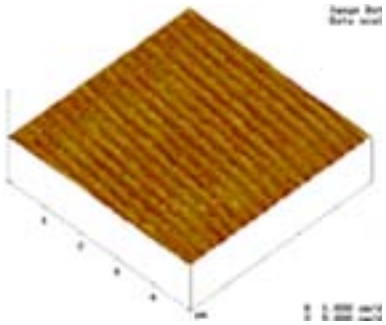

Figure 10: Typical SiC CMP surface using AFM

growth has been performed on over 300 wafers. Growth has been successful by both MBE and MOCVD epitaxy. Figure 10 shows a representative example of a CMP-finished 5µm x 5µm area under AFM. Clear bi-layer terraces are consistently visible, whose pitch correspond to wafer orientation in reference to the (0001) plane. Atomic terracing was previously thought to occur primarily only

after high-temperature hydrogen etching [2]. Appearance of these edges has been established as an incoming substrate surface qualifier to epitaxial growth operations at some customers.

CONCLUSIONS

Careful process monitoring and removal of damaged sub-surface crystal in SiC is critical to production of a successful surface ready for homoepitaxial or heteroepitaxial growth. While high-temperature hydrogen etching had previously proven most successful for achieving very low Ra and PV results on SiC and revealing the atomic step edging necessary to properly nucleate SiC homoepitaxy and GaN and other heteroepitaxy, II-VI has proven CMP capable of achieving lower roughness while still revealing bi-layer step edges, and significantly more economically.

In the development of the process, optical interferometry has proven an invaluable tool for process control, damage identification and diagnosis, and final wafer inspection. Lateral resolution does not approach the capability of AFM, but inspections can be done quickly enough to enable the tool's use as an in-situ process characterization tool.

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ACRONYMS

SiC: Silicon Carbide
GaN: Gallium Nitride
CMP: Chemical Mechanical Polishing
AFM: Atomic Force Microscopy
MOCVD: Metal Organic Chemical Vapor Deposition
MBE: Molecular Beam Epitaxy
Ra: Average roughness
PV: peak-to-valley maximum roughness