Uniform InP/InGaAs SHBT Fabrication Using ICP emitter Etching on 4-inch Wafers

Sangmin Lee, Javier Fierro, Sonja Nedeljkovic, Amal Weththasingha, Nguyen Nguyen and Chanh Nguyen

Global Communication Semiconductors, Inc
23155 Kashiwa Court, Torrance, CA 90505
Email: slee@gcsincorp.com; Phone: 310-530-7274 x136

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Abstract

In this paper, we report manufacturable InP/InGaAs HBT fabrication technology using Cl_2 based Inductively coupled plasma etching (ICP) for Emitter mesa formation. For comparison, we also fabricated devices with wet etched Emitter mesa, which is so far GCS's base line HBT process. Dry etched Emitter devices show better uniformity, lower Emitter resistance, higher ft and comparable Emitter Base junction leakage current. The Emitter mesa undercut from SEM pictures was about half of wet etched emitter. This process will lead us to a reliable and reproducible InP HBT process with extreme lateral scaling of devices for ultra high speed IC fabrication.

Introduction

The purpose of this work is to improve uniformity and controllability of Emitter mesa etch process using ICP dry etch technique. We have already developed manufacturable InP/InGaAs HBT process on 4 inch wafers using wet etched Emitter mesa which has ~0.15 μm undercut from each side, which is good for devices with 1 μm Emitter contact width.[1] For further lateral scaling of the devices, however, deep sub-micron Emitter contact and a mesa etch process with tighter undercut control and better uniformity are necessary.

For deep sub-micron Emitter process, dry etching process seems the most probable solution. Several researchers have sucessufully demonstrated dry etched emitter HBT process using $CH_4/H_2/Ar$ RIE for InAlAs/InGaAs HBT with Be dopped Base layer [2] and BCl_3/N_2 RIE for InP/InGaAs HBT with C-doped base layer. $CH_4/H_2/Ar$ etch, however, shows severe H2 passivation effect on the C-doped base layer. Also BCl_3 or Cl_2 based RIE at room temperature shows etch damage of ion bombardment as well as $InCl_2$ micromasking which makes the surface rough or followe up wet etch to be difficult or not reproducible. To prevent this problem, low power ICP etch at elevated substrate temperature is highly desirable.

This paper is the first successful demonstration of high temperature Cl_2 based ICP emitter etch process of InGaAs/InP HBTs on a 4 inch substrate. To confirm its superior uniformity and device performances, the data of wet etched devices on a 4-inch wafer with the same epi structure will be compared side by side to those of ICP etched devices.

Device Fabrication

We used GCS's base line HBT process and standard epi structure except Emitter dry etch process. For Emitter dry etch, we used STS ICP with high temperature option, which can raise the substrate temperature up to 200 C. This equipment has been proven for vertical InP etching with smooth and clean sidewall. [4] To minimize the etch damage of ion bombardment, we used a low platen power. After a series of experiment, the etch condition was optimized to make smooth and vertical sidewall as shown in fig.2 (a). The ICP etch stopped using 670 nm wavelength Intellemetrics laser end point detector. (LEPD) We stopped etching at the 2nd minimum of 1st derivative of reflected light signal as shown in the fig. 1. In this way we could stop etching consistently at an intended position.

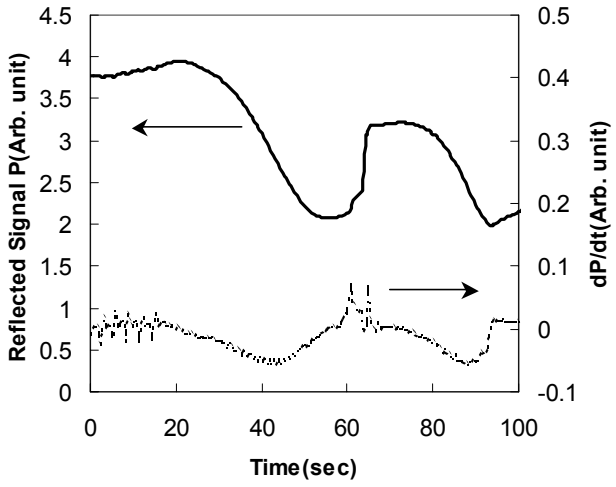

Fig. 1 Laser end point signal (solid line) and its 1st derivative (dotted line) from Cl_2/N_2 ICP etch

After ICP etching, InGaAs and InP selective wet etching were followed. Figure 2 shows the cross sectional view of Emitter mesa before (a) and after (b) wet etching. It shows vertical sidewall of dry etched Emitter and small undercut after wet etching.

The rest of the process after Emitter mesa etch is exactly same to GCS's base line InP HBT process which includes non self-align base contact, base mesa wet etching and BCB passivation and planarization. So the wet etched emitter mesa devices and dry etched one were merged after Emitter mesa process step and followed exactly same process sequence at the same time.

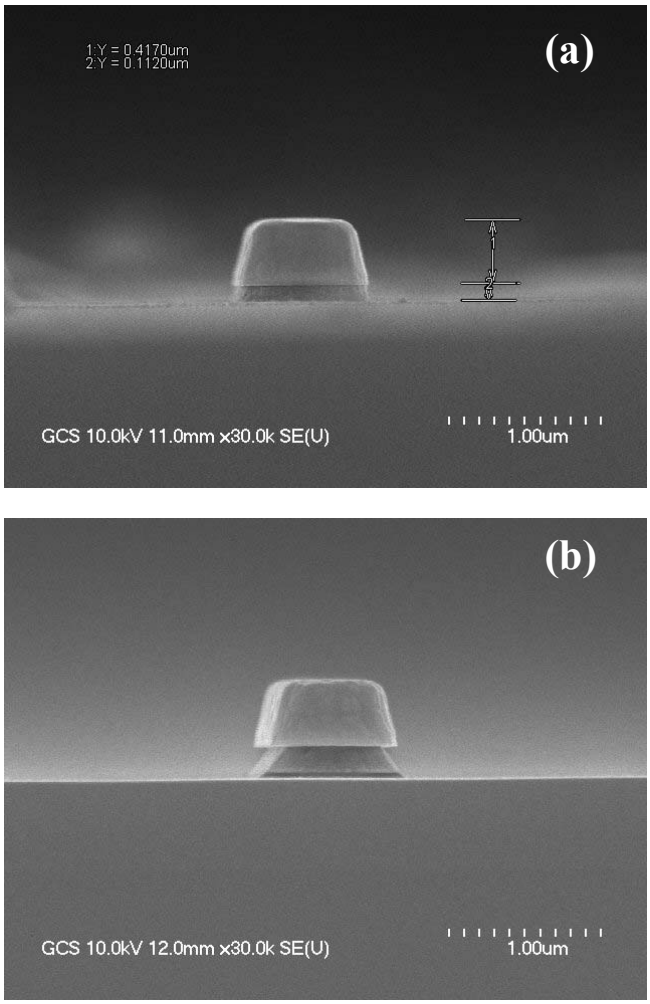

Fig. 2 Cross-sectional view of Emitter mesa (a) right after ICP etch and (b) InGaAs/InP selective wet etch

RESULTS

Fig 3 shows the averaged Gummel plot of wet and ICP etched devices over the whole 4-inch wafers. We measured the devices with 1x3 μm^2 Emitter contact dimension from 38 sites. We have device yield of 84.2 and 92.1 % and DC gain of 42 ± 5.3 and 44 ± 1.6 for wet and ICP etched devices respectively. The standard deviation of DC gain of ICP etched devices is 1.6 which is much less than 5.3 of wet etched ones indicating the uniformity of ICP etched devices is much better than wet etched. The device characteristics calculated from Gummel plots and reverse leakage current (I_r) of Emitter Base junction are summarized in Table 1.

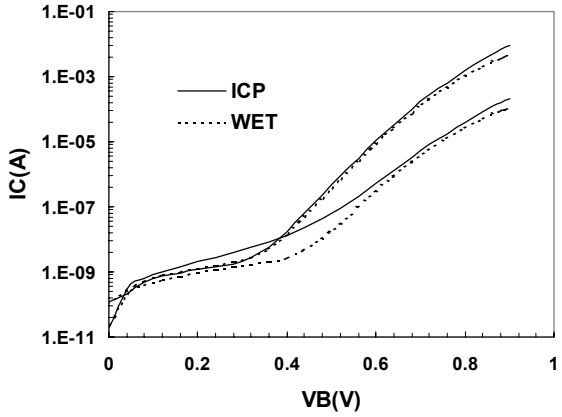

Fig.3 Averaged gummel plot of Wet (dotted line) and ICP (solid line) etched devices.

Table 1. Averaged device characteristics such as DC gain measured at V_B=0.9 V, ideality factor of Base Collector junction (η_C) and Emitter Base junction (η_B) and reverse leakage current (I_r) of Emitter Base junction measured at –3 V bias.

Devices	Gain	η_C	η_B	$I_r(\mu A)$
ICP	44±1.6	1.28	1.65	4.0
Wet	42±5.3	1.28	1.48	2.9

The Emitter resistance estimated from the slope of I_B vs V_C characteristics shown in figure 4 are 19.5 ± 1.3 Ω for ICP etched devices and 25.8 ± 3.0 Ω for wet etched. The reason of smaller Emitter resistance is the smaller Emitter mesa undercut of ICP etched devices. Because of this smaller Re, we measured a little higher f_t from ICP etched devices as shown in fig.5. The f_t of ICP and wet etched devices are 201 ± 2.4 GHz and 177 ± 4.5 GHz.

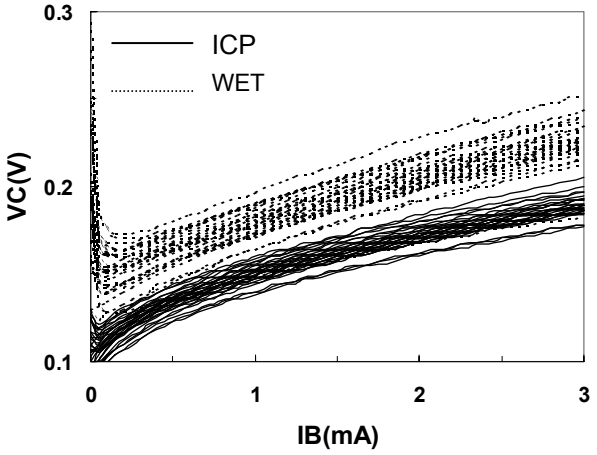

Fig.4 VC vs IB characteristics of ICP etched (solid lines) and Wet etched (dotted lines) devices.

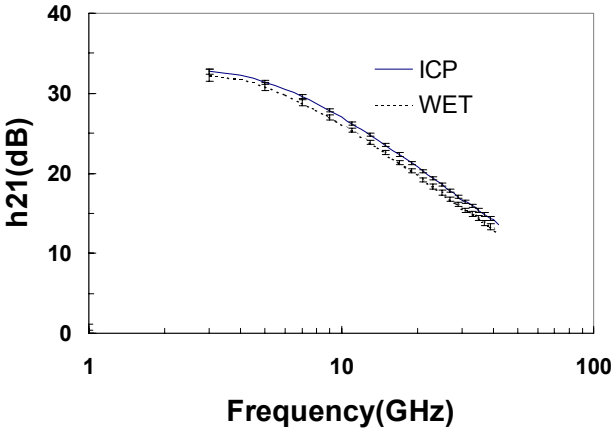

Fig 5. Averaged h_{21} for ICP (solid line) and Wet (dotted line) etched devices at V_C=1.2 V and J ≈ 300 kA/cm^2.

CONCLUSIONS

We have demonstrated InP/InGaAs HBT using a Cl_2/N_2 based ICP etching technique for Emitter mesa formation on 4-inch wafers. We measured small mesa undercut which is about half of the undercut measured from wet etched devices. We developed uniform ICP Emitter etch with accurate etch end point control. We measured higher yield, better uniformity, lower Re and higher f_t for ICP etched devices compare to wet etched ones. This technique may lead us to a manufacturable IC fabrication with deep sub-micron laterally scaled InP/InGaAs HBTs.

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ACRONYMS

HBT: Hetero-junction Bipolar Transistor
ICP: Inductively Coupled Plasma
LEPD: Laser End Point Detector
GCS: Global Communication Semiconductors