Low Temperature High Density Highly Uniform Si_3N_4 Technology for Passive and Active Devices in MMMIC Applications

K. Elgaid, H. Zhou, C.D.W. Wilkinson, I. G. Thayne
Nanoelectronics Research Centre, Department of Electronics and Electrical Engineering
University of Glasgow, Glasgow, G12 8LT, Scotland, United Kingdom
Phone: + 44 141 330 6678, Fax: + 44 141 330 4907, e-mail: kelgaid@elec.gla.ac.uk

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Abstract

In this work a novel, high quality, high-density, 100% yield, deposited at room temperature ultra thin 5nm Si_3N_4 Metal Insulator Metal (MIM) capacitor process for Monolithic Millimetre-wave Integrated Circuits (MMMICs) applications is demonstrated using inductively coupled plasma enhanced chemical vapor deposition technique (ICP-CVD). Capacitance of 6.7fF/µm^2 and a breakdown electric field of more than $3x10^6$Vcm^{-1} were achieved. RF characterisation and equivalent circuits models were extracted which showed an increase in capacitance per area by more than thirteen fold and reduction in RF loss as silicon nitride thickness reduced from 120nm to 5nm. Comparison with high temperature conventional 300°C PECVD Si_3N_4 was also investigated, a comparable breakdown voltage, and leakage current was observed. We also present DC and RF results on 70nm T-gate SiGe MIS gate MODFETs using novel Si_3N_4 deposited at 22°C and lift-off techniques gate dielectric contact and its performance compared with devices made on the same chip using standard Schottky contact. This 5 nm Si_3N_4 gate dielectric enhanced the performance of gate leakage current and breakdown voltage.

INTRODUCTION

A thin layer of Si_3N_4 is an essential element in realising MMMICs. Passive components requiring Si_3N_4 such as MIM capacitors are widely used for filtering, dc blocking, matching circuits, and biasing circuits in MMMIC technologies [1]. Si_3N_4 is also used for passivation, and planarisation, and reducing the effective length of transmission lines [2- 3]. Therefore Si_3N_4 thin film deposition conditions, reliability and reproducibility are important issues for MMMICs viability.

Currently, Si_3N_4 used in MMMIC realisation is based on PECVD deposited at 300°C. This process has proven to be reliable in MMMIC technology but it has the disadvantage of high temperature deposition environment. The high temperatures may result in active layer damage or ohmic contact and Schottky contact degradation, and therefore Si_3N_4 layer deposition must be performed early in the overall process flow, reducing the flexibility of the fabrication process cycle.

Low temperature deposition gives an extra freedom to use MIM capacitors on substrates sensitive to high temperature or the flexibility to realise passive elements fabrication after active devices have been completed, leading to "sea-of-gates" possibilities for mm-wave applications.

The advantages of ultra thin MIM capacitors include the ability to realise very large capacitors values in a smaller area which reduces the parasitic inductance and RF losses, and miniaturisation in wireless systems allow greater integration, lower power consumption, reducing weight, and cost.

RESULTS

The leakage current and the breakdown voltage of Si_3N_4 capacitor deposited at 22°C using ICP-CVD techniques is found to be similar to that based on capacitors with a PECVD Si_3N_4 Insulator deposited at 300°C as shown in Figure 1. From figure 1 we observe that a breakdown electric field of greater than $3x10^6$ Vcm^{-1} was achieved using the novel room temperature deposited Si_3N_4.

Figure 2 shows the leakage current of a 200µm^2 area 5nm thin film Si_3N_4 capacitor deposited at 22°C using ICP-CVD. Leakage current of less than 50nA at 2V was observed, indicating both high quality films with low pin-hole density, and good conformal coating as the nitride film has successfully covered a step of 150nm, the thickness of the lower capacitance plate, without significant additional leakage. Capacitance values were extracted from RF measurements up to 60GHz as shown in Figure 3 which shows the extracted capacitance and the equivalent circuit model used for series capacitors of 5nm and 120nm thick Si_3N_4 deposited at 22°C using ICP-CVD. The capacitance of the 5nm thick Si_3N_4 showed an increase of more than thirteen fold in value, it also showed less inductance and RF loss. From the data in Figure 3, a relative permittivity of 7.5 was extracted for the low temperature deposited nitride films.

Figure 4 compares the output characteristics (a) and gate leakage current (b) of 70nm T-gate SiGe MODFETs using 5nm novel room temperature deposited Si_3N_4 gate dielectric contact and compared with that of Schottky contact. It is observed that a smaller gate leakage current is exhibited by the MODFETs with 5nm novel room temperature deposited Si_3N_4 gate dielectric than that of the Schottky contact as shown in figure 4b. Figure 5 shows f_T of a 70nm T-gate SiGe MODFETs using 5nm novel room temperature deposited Si_3N_4 gate dielectric contact (a) and compared with that using a Schottky gate contact (b). f_T of 51GHz and 65GHz was observed respectively. A lower f_T of the Si_3N_4 gate dielectric contact devices could be due to the un-optimised layer structure.

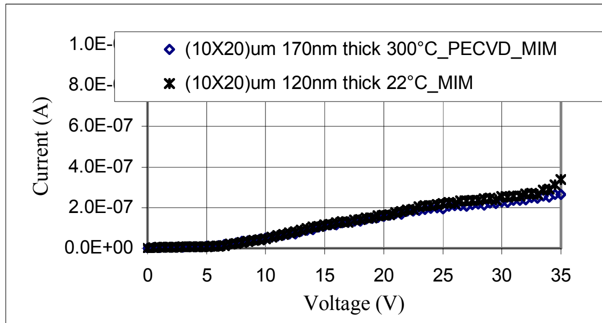


Figure 1 – Leakage current of a 200µm^2 120nm thick Si_3N_4 capacitor deposited at 22°C using ICP-CVD compared to that of a 170nm PECVD deposited at 300°C

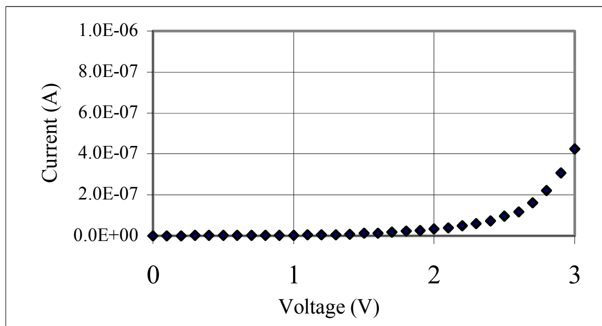
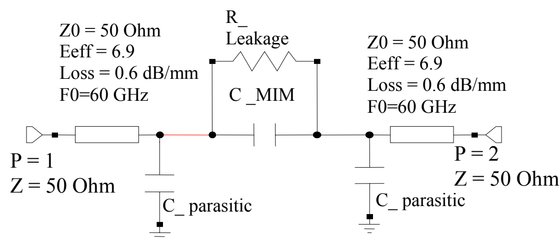


Figure 2 - Leakage current of a 200µm^2 area 5nm thin film Si_3N_4 capacitor deposited at 22°C using ICP-CVD



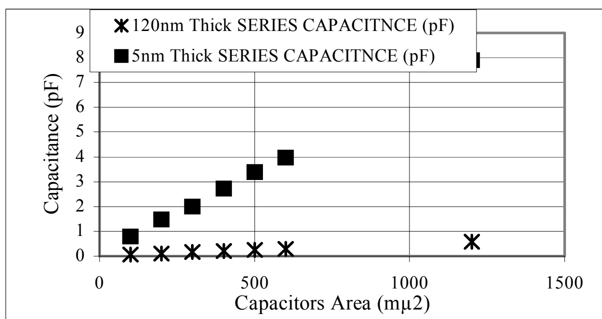
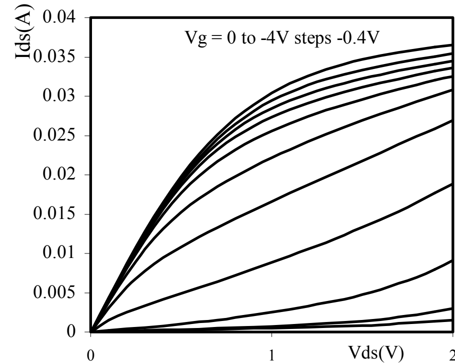
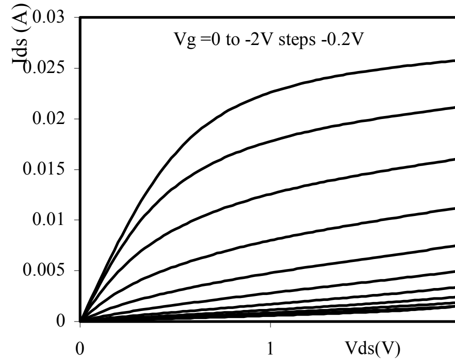


Figure 3 – Capacitance values as a function of capacitors area extracted from RF measurements of a 5nm and 120nm thick Si_3N_4 deposited at 22°C using ICP-CVD, equivalent circuit model used is shown above plot.



Output characteristics of 70nm T-gate SiGe MIS gate MODFETs



Output characteristics of 70nm T-gate SiGe Schottky contact MODFET

Figure 4 (a)

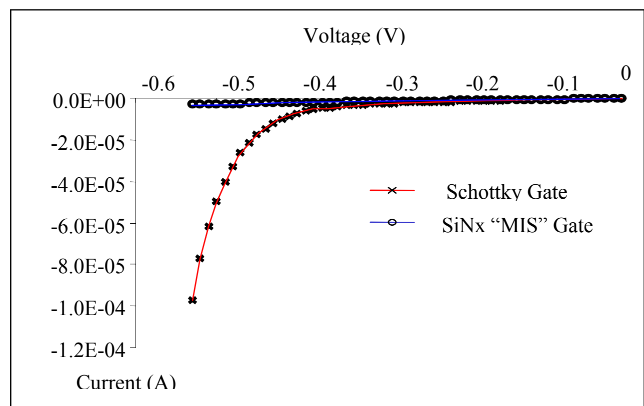


Figure 4 (b)

Figure 4 Compares the output characteristics of 70nm T-gate SiGe MODFETs using 5nm novel room temperature deposited Si_3N_4 gate dielectric contact and compared with that of standard Schottky gate contact (a) and gate leakage current of 70nm T-gate SiGe MODFETs using 5nm novel room temperature deposited Si_3N_4 gate dielectric contact and compared with that of standard Schottky contact (b)

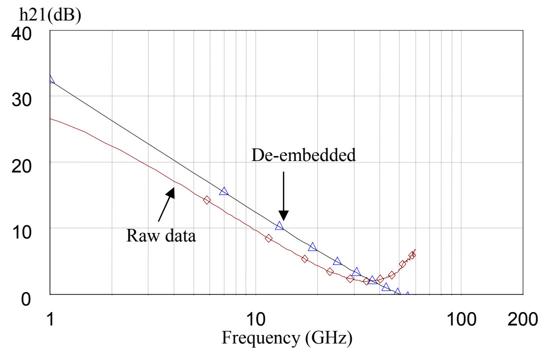


Figure 5 (a)

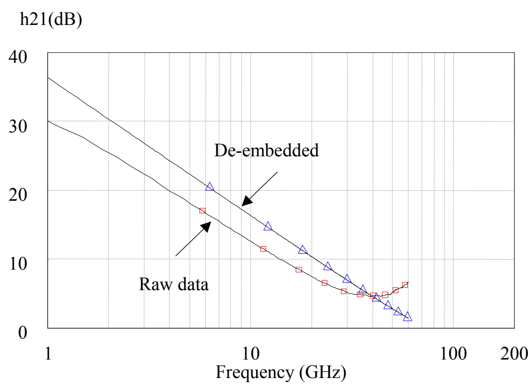


Figure 5 (b)

Figure 5 Compares RF performance of 70nm T-gate SiGe MODFETs using 5nm novel room temperature deposited Si_3N_4 gate dielectric contact (a) with that of standard Schottky contact gate (b)

CONCLUSIONS

A novel, ultra thin, 5nm room temperature Si_3N_4 deposition techniques based on ICP-CVD for MMMICs technologies has been realised. The fabrication process requires only one step lithography followed by dielectric deposition and lift-off, unlike the currently used 300°C PECVD process where additional steps of lithography and dry etching are required. The new capacitance process showed 100% yield with high uniformity across the wafer. Large capacitance values of 6.7fF/μm^2 and a breakdown electric field of more than $3x10^6 Vcm^{-1}$ were observed. In comparison with existing 300°C PECVD Si_3N_4 process, the new process offers: reduced thermal budget, comparable leakage current, comparable dielectric constant, greater than thirteen fold in capacitance per unit area could be achieved using ultra thin films with leakage current of less than 50nA at an applied voltage of 2 Volt.
Active devices been realised using this novel ultra thin 5nm room temperature Si_3N_4 as a gate dielectric and compared with that of Schottky gate contact. Comparison of RF results for both devices is presented.

ACKNOWLEDGEMENTS

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