# Continuous Defectivity Improvements and Impact on High Density Metal-Insulator-Metal (HDMIM) Capacitor Yields

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**Abstract**

**Motorola's continuous improvement methodology and focus on defectivity has paid significant dividends in the form of record wafer yields and in particular record High Density Metal-Insulator-Metal (HDMIM) capacitor yields. The institution of a defectivity program has identified defect generators within the process flow and efforts to reduce defectivity at the sputtered layer of the bottom plate and evaporated layer of the top plate HDMIM capacitor formation are reported. Addition of process controls at both the bottom and top plate processes to monitor and reduce defectivity are discussed. These process controls include, the modification of a MRC sputter tool, chemical clean of incoming Au pellets and the addition of tantalum to the gold for the evaporation process. A ten time improvement in defect reduction at the bottom and top plate of the HDMIM capacitor has been realized and the impact on yields is reported. The reductions in defectivity have allowed Motorola's CS1 to calculate intrinsic reliability in excess of our corporate goal.**

## INTRODUCTION

In 2001, Motorola's CS1 GaAs manufacturing facility challenged traditional beliefs that a defectivity program in a GaAs facility did not make good business sense and instituted a defectivity program in an effort to reach record yields for devices using HDMIM capacitors. The HDMIM capacitor utilizes a thinner dielectric than the standard planar capacitor. This was commercially attractive from a die-cost perspective since designs utilizing the HDMIM capacitor could be made smaller due to the smaller capacitance per unit-area offered by the new design. A cross-sectional description of the HDMIM capacitor is shown in Figure 1.

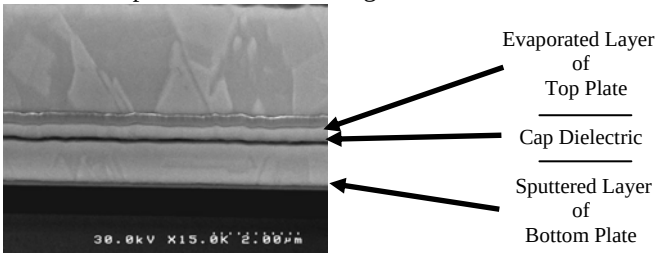


Figure 1 – Cross Section of HDMIM Capacitor

## CAPACITOR BOTTOM PLATE DEFECTIVITY

Failure analysis of poor yielding wafers showed that capacitor failures in the form of low breakdown at parametric test were due to particulates in or under the metal-1 film. These particulates disturb the deposition and subsequent integrity of the silicon nitride dielectric causing a short when the next metal layer, metal-2, is deposited as shown in figure 2. The defectivity team executed to a comprehensive and intensive evaluation plan, which included a base line measure of defectivity in the HDMIM capacitor module, to identify high sources of defectivity. Although all process tools within the HDMIM capacitor module were under investigation as possible defect contributors, the frequency and severity of the defect shown in figure 2 was deemed as the most critical defect in terms of its obvious ability to affect capacitor yield. This particle originating at the seed layer suggested that its source was the metal-sputter tool used to deposit the titanium adhesion and gold seed films. This particle acts as a nucleus during the metal-1 plating process causing an extrusion of the metal-1 bottom-plate of the capacitor. This extrusion is too-tall for the thin capacitor dielectric to cover or insulate, which results in a direct electrical short between metal-1 and metal-2 when the subsequent top-plate of the capacitor is deposited.

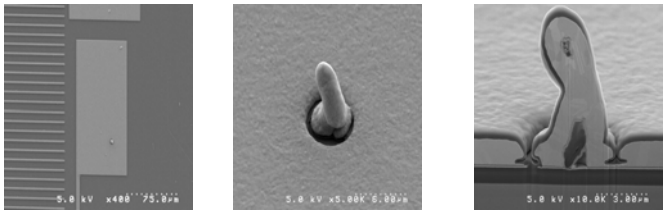

Figure 2 – Particle Resulting in Failing Capacitor

The biggest benefit in critical defect reduction came from moving the gold seed deposition process from an older generation MRC sputter tool to a newer generation MRC sputter tool. In addition, these tools were retrofitted with a 'defect catch plate' below the gate valve and reprogrammed so the soft-vent and purge features of the load-lock would

function with the optimum 'back-draught' so as to not disturb particulates onto the wafers. Shiftly load-lock wipe-downs and subsequent particle checks were also introduced in an effort to keep the tools free from defects. Cleans and particle checks on the tools were scheduled through an automated system and SPC charts were implemented to record and monitor the defect levels of all tools in the capacitor module. Those efforts are reflected in the decreasing defectivity trend and increasing yield trend shown in figures 3 and 4 respectively.

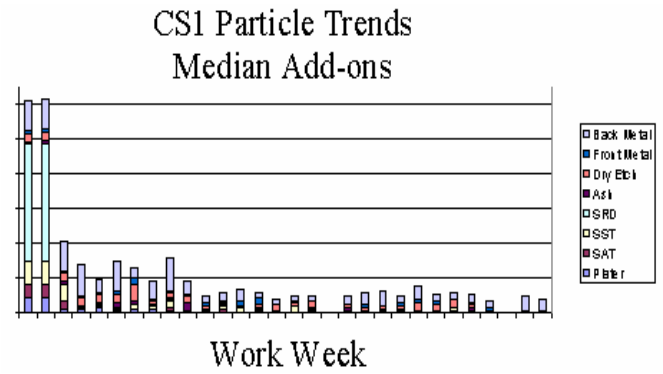


Figure 3 – CS1 Particle Trends

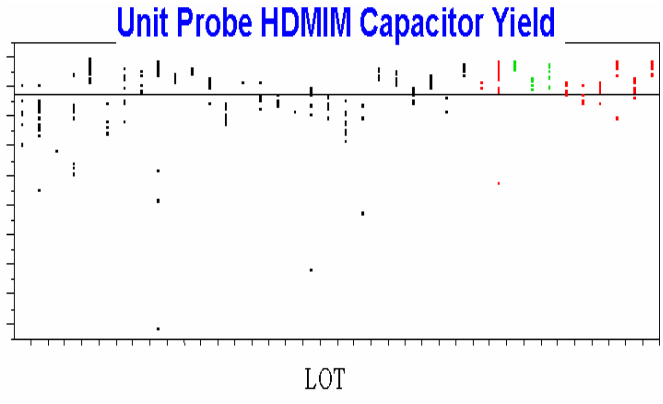


Figure 4 – Capacitor Yield Trends

## CAPACITOR TOP PLATE DEFECTIVITY

The direct correlation between improved capacitor yields and the defectivity program resulted in a paradigm shift through out the engineering community. As defectivity monitors were made more robust through out the factory, new opportunities for improving yields became evident. A new inline defectivity process monitor, using a dark field microscope lens, identified our evaporated metal process as a significant contributor to defectivity where as our traditional defectivity checks, which used bare silicon monitors to check the defectivity of the handling system did not. Furthermore, given the percentage of wafer area occupied by capacitors, the number of these defects present per $cm^2$ was consistent with recent yields.

Cross-sectional and elemental analysis of defects from failing capacitors identified spherical gold artifacts in the capacitor layers, shown in figure 5 and 6, as a potential cause of yield loss. The shape of the defect indicated that as the

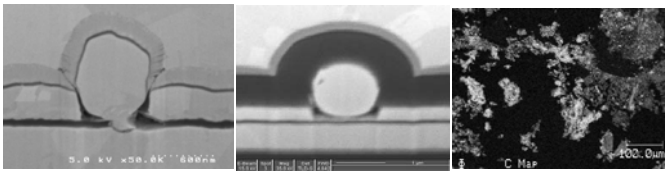

Figure 5 - Gold Defect Figure 6 – Gold Defect Figure 7 – Carbon Map

gold was evaporated, it would also 'spit' or eject spheres of molten gold. An analysis of the surface of the gold source in the evaporator identified carbon contaminants, shown on the carbon map in figure 7. When the carbon was wiped from the surface of the gold source, the defectivity level significantly decreased proving that the carbon was the spitting catalyst. However, after each process run the carbon residue would return to the surface of the gold source and defectivity levels again increased. The tool was thoroughly examined for the source of the carbon and was ultimately traced back to the incoming gold pellets. As a result, an incoming gold pellet cleaning procedure was developed to remove surface contaminants, which consisted of an ultra sonic alcohol and acetone bath followed by a hydrogen peroxide bath and water rinse. When this clean was implemented in conjunction with wiping the carbon reside off of the gold melt prior to each run, the defectivity level was reduced by five times and yields improved but with high variation.

The variation in yields was most probably a result of the trace amounts of carbon coming from with in the gold. Once the gold pellets, which are added to the source after every run, have been 'burned in' or melted into the source, the carbon is released from with in the pellet and collects on the surface of the gold source. The solution to this issue was the addition of tantalum to our evaporated gold source. Since tantalum is less dense than gold, it floats on the surface and acts as a getter absorbing carbon from the gold [1]. In addition, tantalum has a higher evaporation temperature than gold and therefore will not evaporate during gold deposition. Over time, the carbon rich tantalum slowly wicks over the side of the crucible. Periodically, the tantalum in the gold must be replenished and the outside of the crucible must be cleaned to remove the tantalum build-up. The introduction of tantalum to our gold evaporation process resulted in an immediate reduction of variation in defectivity and record yielding wafers shown in figure 8.

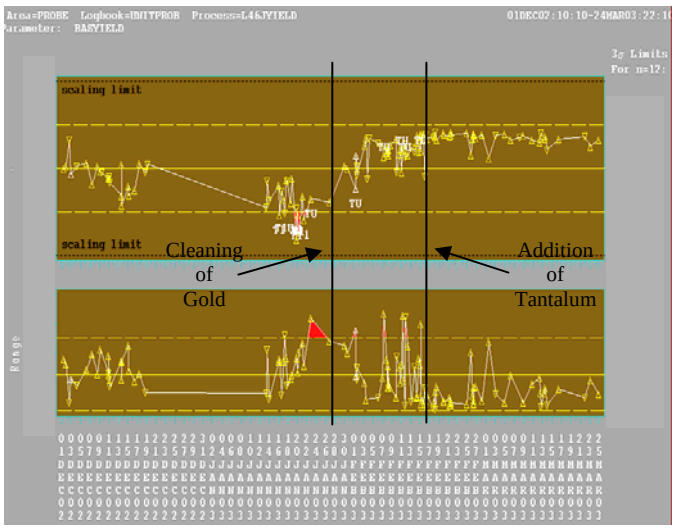


Figure 8 – Wafer Yield Trends

Due to the extremely sensitive nature of this evaporated layer, the need for real time defectivity monitoring was obvious. The solution was to convert from a traditional bare silicon defectivity monitor measured on a Tencor Surfscan to an evaporated production film measured on a KLA 7600. Data from defectivity monitors that ran with every production lot was collected over a period of time and correlated to probe yield with an $R^2$ = .72 as shown in Figure 9.

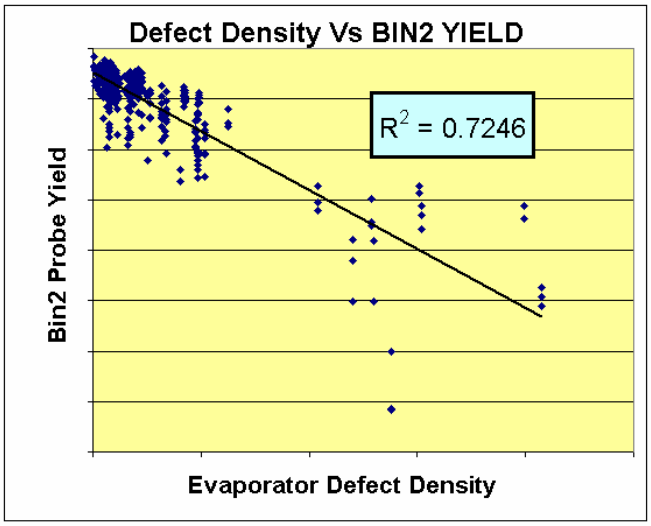


Figure 9 – Process Monitor Vs Yield Correlation

The correlation between the process defectivity monitor and wafer yields provided the factory with a tremendous cost avoidance tool. Production material that measures high defectivity during processing is now scrapped immediately rather than incurring additional processing costs only to find that the yields are poor at final test. In addition, the process defectivity monitor allows real time feed back on process control rather than relying on parametric test at the end of the flow.

## INTRINSIC RELIABILITY

As part of Motorola's on-going reliability improvement and focus on a zero defect initiative to our customers, the defectivity and subsequent yield improvements achieved were scrutinized for intrinsic reliability or IR performance. The objective of this initiative was to evaluate the performance of a HDMIM capacitor as used within a power amplifier application. This was facilitated through Time Dependent Dielectric Breakdown or TDDB [2] and Voltage Ramp Stress or VRS testing [3-4] of a HDMIM capacitor under conditions deemed worst case in terms of environment and application. These conditions were extensively modeled on an application-specific basis and determined to be 18V and 70C for the standard HDMIM capacitor used in our standard production flow. Over 200 samples were used for the TDDB test to provide a statistically significant sample of data and extrapolation techniques proved that the VRS method was compatible with the TDDB test method used in this evaluation. The VRS test is a much shorter test than the time-consuming TDDB test, thus demonstrating the attraction of having both of these tests compatible in terms of their data output.

Results of the IR evaluation on the improved process showed the capacitors to have a field-use life, under worst case operating conditions, in excess of 10 years. The obvious ancillary benefits of this level of testing are the development of the VRS method to test such passive components in a comparatively short time and the ability to quickly respond to any defect issues and subsequent failure analysis required. This will provide a benchmark method of assessing the IR of the HDMIM capacitor in the event of any future processing anomalies or yield excursions

## CONCLUSIONS

The defectivity program instituted at CS1 has been invaluable to the organization by uncovering a variety of process improvement opportunities with respect to defectivity. Tool modifications at the seed layer of the bottom plate of the capacitor and the addition of tantalum to the gold source at the evaporated layer of the top plate of the capacitor have reduced defectivity by 10 times at each of those processes. As a result, CS1 has reached record HDMIM capacitor and wafer yields. The addition of improved defectivity process monitors, which correlate to wafer yields with an $R^2$ = .72, ensures process control with respect to defectivity and provides the engineering community with a powerful cost avoidance tool. Finally, a time efficient comparative method of Intrinsic Reliability monitoring in the form of VRS testing has been devised. The collection of benchmark data on the HDMIM Capacitor will lead to implementation of a method to further investigate any future extrinsic reliability excursions as well as provide on-going

Intrinsic Reliability insurance. Motorola's CS1 will continue to monitor defectivity levels using SPC at both bottom and top plate formation of the capacitor and look for continuous improvement opportunities. This continued focus on defectivity will allow Motorola's CS1 manufacturing facility to continue to enjoy record yields while improving cost and quality for our customers

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## Acronyms

HDMIM: High Density Metal-Insulator-Metal
IR: Intrinsic Reliability
TDDB: Time Dependent Dielectric Breakdown
VRS: Voltage Ramp Stress