Novel Via Planarization Scheme for High Resolution Backside Wafer Processing

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***Abstract*–Backside wafer planarization methods are discussed in GaAs substrates. First method uses an epoxy based polymer to fill 10 mils deep via structures while the second method demonstrates a solidly filled 3.5mils deep metal vias. The planarization step is accomplished with a lapping and polishing step which exposes the via connection to the frontside. As a result high definition photolithography is made possible on the backside of the wafer normally compromised by the existence of the via structures. A monolithic circuit is fabricated with greater than 10mil deep via structures. The circuit is planarized using the epoxy technique and electrical contact is made through stripes in the frontside of the wafer. Streets separated ground and signal paths on the backside of the wafer connecting to large area solder bumps. The latter allows successful backside biasing of the frontside circuit with a planarized surface.**

***Index Terms*— Substrate Via, Electomagnetic Crystal technology (EMXT), Inductively coupled plasma etching (ICP), planarization, Source via, PHEMT, power amplifiers, MMICs**

I. Introduction

As the application of microwave and millimeter wave products become increasingly more complex, integrated system solutions are required for improving performance criteria. This reduction in system size and space requirements filter through to the component levels and provide demanding challenges to already complex fabrication processes. On such application is the electronically steered antenna technology which has seen novel assemblies where the active devices are incorporated in the antenna itself [1,2,3,4]. As a result, multi layer circuit topology might need to be developed to take advantage of closely coupled antenna elements. In this paper we describe a method by which the backside of the GaAs MMIC wafer could be used for high resolution lithography after a novel substrate via planarization process. This in turn will add additional functions to the MMIC such as backside biasing capability through solder pads.

Generally the MMIC circuits are designed in microstrip or grounded coplanar waveguide structures which require substrate vias to the ground on the backside of the wafer. Once these via structures are fabricated the backside of the wafer has deep voids which result in uneven lithography and hamper line resolution. For example if additional solder bumps are required the larger size solder bumps would need to overlap with the deep vias and any trapped photoresist might eventually outgas and cause a reliability issue. Two methods are described in this paper in order to eliminate the latter and regain the high resolution lithography. First method is mainly targeted for via depths in excess of 3.5mil which include an epoxy filled steps for planarization process. The second method targets smaller dimension and depth vias and planarizes the via structures by a solid electroplated metal layer. This process also provides a better heat transfer when used for high power MMIC applications [5,6,7].

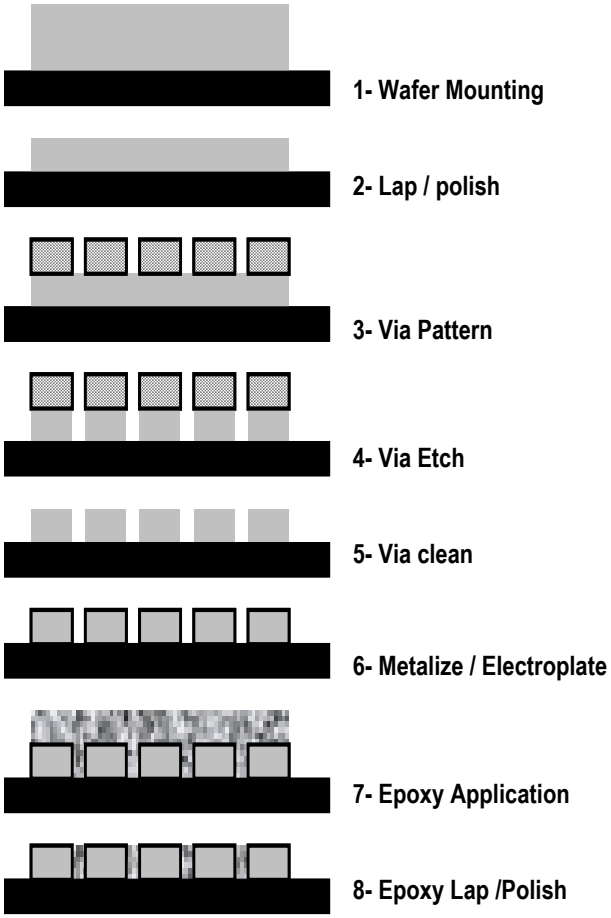

Figure 1- Schematic representation of the epoxy Planarization process

II. Epoxy Planarization Process

Figure 1 shows the process flow diagram of the via planarization scheme based on an Epoxy layer. The GaAs wafer is mounted using low temperature wax on a larger sapphire carrier. The wafer is then measured, lapped and polished using lapping compounds to 10.5mils thick. The via mask is then patterned into a 25um thick photoresist which is hard baked after DUV post exposure to conserve its pattern contrast. The via etch process is then carried out using an Inductively coupled plasma (ICP) assisted dry etch process to etch through the via pattern and arrive at the frontside metalization pad. The etch process is a BCL_3, Cl_2 and HB_r chemistry capable of greater than 2.5um/min etch rate for depths of 10mils through the via mask. The uniformity of the etch depth across the 4" wafer is 5% with the outer regions of the wafer etching faster than the inner parts. As a result, an over-etch is performed to complete the etch uniformly across the wafer using the high etch selectivity between the GaAs and metal layers.

The wafer is then cleaned in a hot solvent solution to remove the etch polymer present in the via as a result of the dry etch process and remove the photoresist mask layer. At this point the vias have been opened through to the frontside of the wafer with a slope of 75 degrees replicating the original size of the mask via on the frontside which is 5mils in diameter. The wafer is then sputtered with a layer of Ti/Au metalization. This acts as a continuous seed layer for the consequent step of 3um thick gold plating. The latter provides low resistive contact between the frontside and backside of the wafer.

At this stage the wafer has greater than 11mils deep vias to the frontside of the wafer. Any subsequent photolithography steps will be compromised by the deep via recess where the resist will flow into the via and will not be developed when exposed. In order to perform a high resolution photolithography the vias would need to be planarized

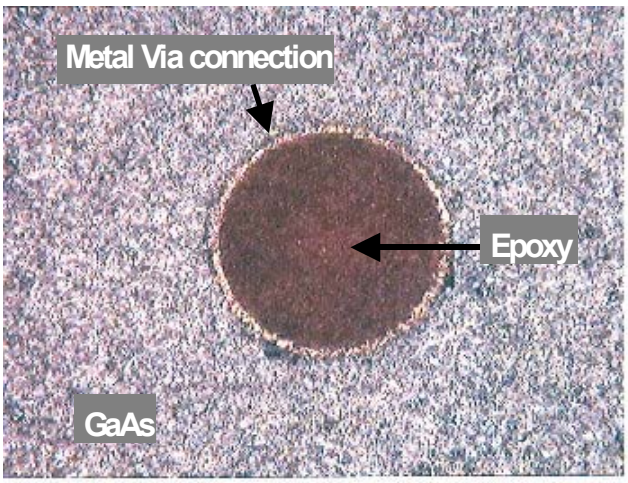

Figure 2- Photograph of a 10 mils deep Epoxy planarized Via in GaAs

resulting in a more uniform photoresist thickness on the wafer. The planarization process uses an organic EpoTek epoxy based polymer which is mixed by weight and applied on the wafer. All the trapped bubbles are removed by applying low pressure outgas vacuum process. The wafer is then baked to cure the epoxy at 100C for 3hours. This is then followed by a lap and polish process step to remove the excess epoxy, the sputtered and plated gold layer from the surface of the wafer. During the above processes the wafer is mounted flat therefore it can be planarized accurately during the process by means of lapping and polishing. Figure 2 shows a photograph of a via after the second lapping process. There are concentric rings where the outer ring is the via etched into the GaAs substrate followed by the metalized ring of the sputtered and plated gold. The final section is the epoxy in the center of the via. At this stage the wafer is planarized including epoxy filled 10 mils vias with extra 0.5mils lost and accounted, for the second lapping and polishing steps. The backside of the wafer can now be used for high definition photolithography and the vias can be electrically contacted to by the metal ring as discussed later.

II. Metal Via planarization Process

Although the epoxy filled via technique would be suitable for all via dimensions and heights a solid metal via could provide not only a low resistive path from the frontside but also a more efficient heat sink. As a result an experiment was devised in order to solidly fill a 3.5mil via pattern through GaAs. The thickness of the substrate was chosen in order to target the MMIC applications where generally the substrate thickness does not exceed 3.5mils. The process follows similarly to the epoxy based process described above in mounting, lapping and defining the via pattern and dry etching chemistry. The lapping thickness is 3.5mils and the via mask size is 50um in diameter. The dry etch recipe is less aggressive with the chamber pressure since the target depth is

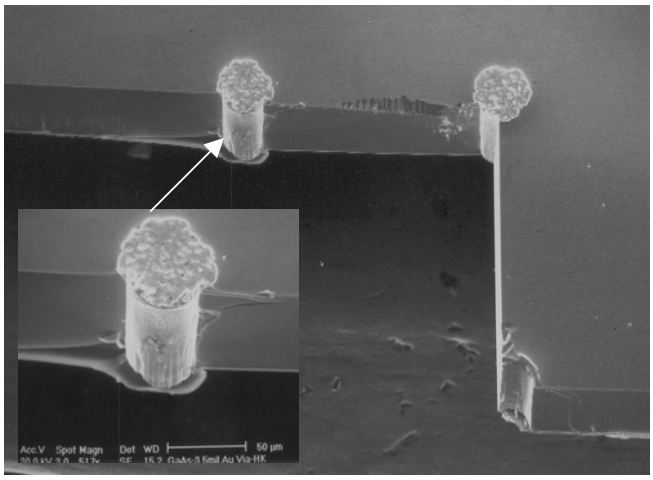

Figure 3 – SEM photograph of solidly filled gold via structures in GaAs

lower. Once the vias have been etched and arrived at the frontside gold layer, the wafer is prepared for electroplating with no seed layer. Since the frontside of the wafer has a continuous layer of metal the vias can be plated if contact is made to it. In this case the GaAs substrate will act like a mask and guide the electroplating through the via structure. The

gold electroplating solution used is a commercially available "Technic 25E" capable of unstressed macro-plating with a smooth finish. Based on the area used the lowest current density was used in order to build up layer in the vias structures gradually. This is important since at high current densities the via sidewalls will be plated faster than the center of the via and voids will appear in the via structure. Once the electroplating is completed some of the via structures have electroplated beyond the top part of the surface and in order to planarize the wafer a lap and polish step is added and in the epoxy process. Figure 3 shows the SEM picture of a 3.5mils deep solidly electroplated gold via with a planarized backside surface. It can be seen that the vias are solidly filled with metal and closely resemble the shape of the original etched profile.

III. Backside-Frontside chip interconnect demonstration

On such demonstration for this technology is shown in Figure 4. This chip has metal stripes in the frontside of the wafer where they need to be alternatively biased from the backside of the wafer through 10 mils vias. The chip functions as an electromagnetic crystal (EMXT) designed to perform as a periodic structure with high surface impedance in a waveguide transmission line [8]. As the bias is applied between these fronside stripes a variable surface impedance is created to the impinging electromagnetic field. This feature can be used to electronically steer the beam for compact, low cost and high performance phased array antennas.

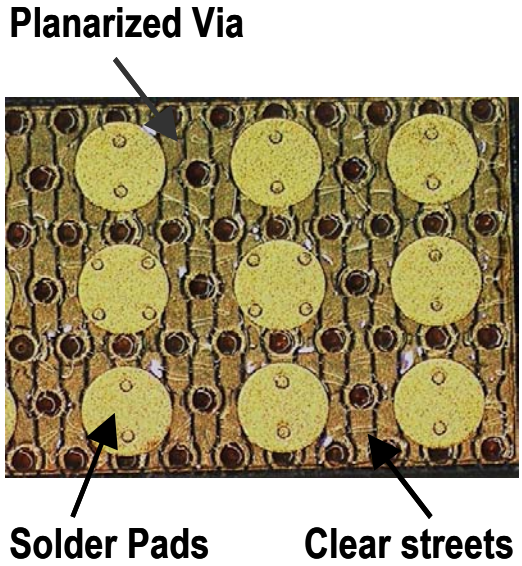

Figure 4 – Backside solder bump technology made available by using epoxy planarized via technology

The chip has stripes loaded with varactor diodes which require bias to vary its surface impedance. The thickness of the chip is a function of its frequency and at Ka-band is 10 mils in depth. The backside biasing scheme used in this case is method described in the epoxy filled via process. Multi-vias are required for each strip to establish perfect signal-ground condition. The common potential via structures are then collected in three larger areas in the backside of the wafer. These areas are separated through streets only 10um wide. In order to define such long 10um line widths across a 7mm chip it is important to have a planarized surface to ensure continuity of the line. The solder pads are then positioned on each area where the chip could be solder bumped on its housing and be controlled completely from the backside of the chip.

IV. Conclusion

An innovative method of backside planarization process has been developed to regain a high resolution backside process lithography and make possible the development of dual faced MMICs and circuits. Two different application specific processes have been employed to planarize via structures of various depths one with epoxy fill with 10 mils and the other solid metal filled with 3.5 mils vias. The process was further demonstrated in a monolithic circuit where bias control to the frontside of the wafer was established by the backside solder bumps made possible by the epoxy based planarization process.

References

[1] Higgins, J.A.; Hao Xin; Sailer, A.; Rosker, M.; "Ka-band waveguide phase shifter using tunable electromagnetic crystal sidewalls" Microwave Theory and Techniques, IEEE Transactions on , Volume: 51 , Issue: 4 , April 2003 Pages:1281 - 1288

[2] M. E. Davis, "Space Based Radar Core Technology Challenges for Affordability," *2001 Core Technologies for Space Systems Conference Dig.,* Colorado Springs, Colorado, Nov. 2001.

[3] McPherson, D.; Bates, D.; Lang, M.; Edward, B.; Helms, D.; Military Communications Conference, "Active phased arrays for millimeter wave communications applications" 1995. MILCOM '95, Conference Record, IEEE , Volume: 3 , 5-8 Nov. 1995
Pages:1061 - 1065 vol.3

[4] Lemons, A.; Lewis, R.; Milroy, W.; Robertson, R.; Coppedge, S.; Kastle, T.; **"**W-band CTS planar array," Microwave symposium Digest, 1999 IEEE MTT-S International , Volume: 2 , 13-19 June 1999 Pages:651 - 654 vol.2

[5] Y. Kwon, D.S. Deakin, E.A. Sovero, J.A. Higgins, "High-performance Ka-band Monolithic Low-Noise Amplifiers using 0.2-µm Dry-Recessed GaAs PHEMTs," *IEEE Microwave and Guided Wave Lett.*, vol.6 no. 7, pp. 253–255 Jul. 1996.

[6] H Furukawa, T Fukui, T Tanaka, A Noma and D Ueda, " A novel Fabrication Process of Surface via holes for GaAs Power FETs", Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 1998. Technical Digest 1998., 20th Annual , 1-4 Nov. 1998 Pages:251 - 254

[7] H. Hendriks, J Crites, G D'Urso, R Fox, T Lepkowski and b Patel, " Challenges in rapidly scaling up backside processing of GaAs wafers" 2001, GaAs Mantech Conf. May21, 2001, p181

[8] Xin, H.; Kazemi, H.; Lee, A.W.; Hggins, J.A.; Rosker, M.J.; **"**Low-loss monolithic tunable electromagnetic crystal surfaces with planar GaAs Schottky diodes" Antennas and Propagation Society International Symposium, 2003. IEEE , Volume: 2, June 22-27, 2003, Pages:435 – 438

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