Advanced InP Heterojunction Bipolar Transistors with Implanted Subcollector

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Abstract

We present the results of an InP HBT device development process. We have developed a new HBT device fabrication approach that represents a major departure from traditional compound semiconductor manufacturing techniques. The new generation of deep submicron InP-based HBTs presented here uses an ion implanted subcollector and offers significantly improved performance, integration, and device reliability over traditional mesa isolated devices. We have fabricated both SHBT and DHBT selectively ion implanted subcollector InP HBT devices with F_t's greater than 260GHz.

INTRODUCTION

Demand for high bandwidth communications systems has accelerated the development of high-speed device technologies including SiGe and InP. Both of these technologies have reported devices with cutoff frequencies greater than 100 GHz. However, most devices with these high performance levels consume too much power for MSI applications. One method of reducing the power consumption in these devices is scale both the lateral and vertical dimensions of the device.

Recently InP HBT devices have been scaled laterally to deep sub-micron dimensions. [1-4] Large area HBT devices have a large ratio of intrinsic to extrinsic parasitics and capable of high ft performance. However, they are greatly limited by excessive distributed intrinsic base resistance. They also dissipate significantly more power than smaller devices for ICs. As mesa transistors are scaled to submicron dimensions, the extrinsic parasitic resistances and capacitances, associated with structures required to contact the intrinsic transistor to the rest of the circuit, become large relative to their intrinsic resistances and capacitances. The result is that submicron scaled HBTs have lower performance compared to larger transistors fabricated with the same process [3].

Epitaxial HBT devices take great advantage of low transit times in the thin layers. Vertical scaling of the epi layers is an effective method of reducing the device transit time but at the expense of increasing both the access resistance and the junction capacitance. Decreasing the base thickness to decrease τ_b increases the base resistance. Decreasing the collector thickness to decrease τ_c increases the base collector capacitance.

BURIED SUBCOLLECTOR

The very thin lightly doped collectors used in many advanced HBT structures are fully depleted even at slight forward bias. This means that the overlap area between the heavily-doped base and subcollector layers outside the intrinsic device adds substantial parasitic capacitance to the device. This capacitance is reduced but not eliminated even in structures that undercut only the collector. [5-7] Patterning the subcollector so that it does not overlap with the base is thus the most important element of extrinsic parasitic reduction. [5]

Eliminating extrinsic parasitics is primarily a processing issue. To minimize the parasitic capacitance associated with base contact/subcollector overlap, we have developed a patterned subcollector by selective ion implantation and regrowth. As in Silicon BJT processing, one way to achieve a buried subcollector is patterned ion implantation to define the subcollector area.

A further limitation of traditional mesa structures is the high aspect ratio which is nearly 3:1 (height:width) even with 0.5μm minimum emitter dimension. This creates physical limitations to the device packing density as well as the length and minimum dimensions of interconnect lines and the yield of integrated circuits. Advantages of the implanted subcollector approach over traditional mesa isolated device processing include:

1) Improved planarity; easing the lithographic requirements for aggressive lateral scaling.
2) Major reduction of the extrinsic parasitic base-collector capacitance (C_{jc}).
3) Improved speed (f_t and f_{max}) primarily from 2 above.
4) Reduced power consumption for the same device speed.
5) Substantial reduction in thermal resistance (R_{th}).

IMPLANTED HBT DEVICE STRUCTURE

In the patterned regrowth technique described here, a masking layer is deposited on the wafer then subtractive processing is used to define the intrinsic device subcollector area. After the wafer is implanted, the implant mask is removed and the rest of the epitaxial layers are re-grown on the wafer over the implanted device areas. In this way, the subcollector is limited to just the areas underneath the intrinsic device and where the collector metal contact pad area.

The buried subcollector HBT device is fabricated by implanting Si into masked S.I. InP substrates. The wafers were implanted at 80keV ($2.5x10^{14}$ cm^{-2}) and 240keV ($5x10^{14}$ cm^{-2}). The implant mask was then removed and the wafers were annealed with a phosphine overpressure at 700 deg. C. The AlInAs/InGaAs/(InGaAs or InP) epitaxial structures described here were grown by GSMBE. All layers were grown lattice-matched on semi-insulating InP substrates and the p-type and n-type dopants were Be and Si, respectively. The basic SHBT structure has been reported elsewhere. [8]

IMPLANTED HBT DEVICE PERFORMANCE

Figure 1 plots the 2-terminal Gummel characteristics of a $0.5x4\mu m^2$ DHBT transistor with an implanted subcollector. Figure 2 plots the DC and AC current gain (beta) of this device. The maximum current gain for the DHBT was greater than 100. These high values of current gain indicate that the base layer was of extremely high quality even though significant wafer processing occurred before the MBE regrowth.

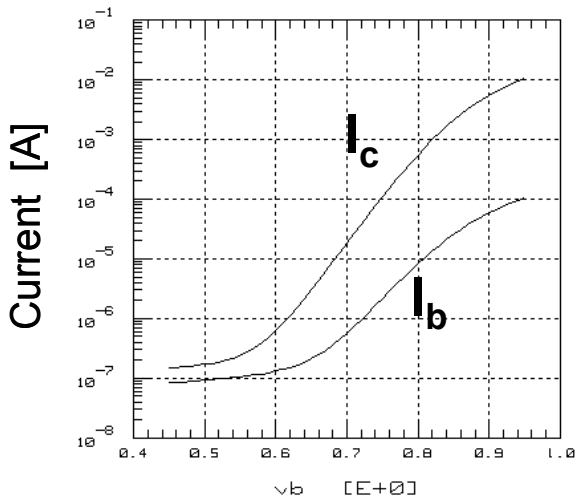

Figure 1.
Measured 2-terminal forward Gummel characteristics of a ion-implanted subcollector DHBT device with emitter area = $0.5x4\mu m^2$.

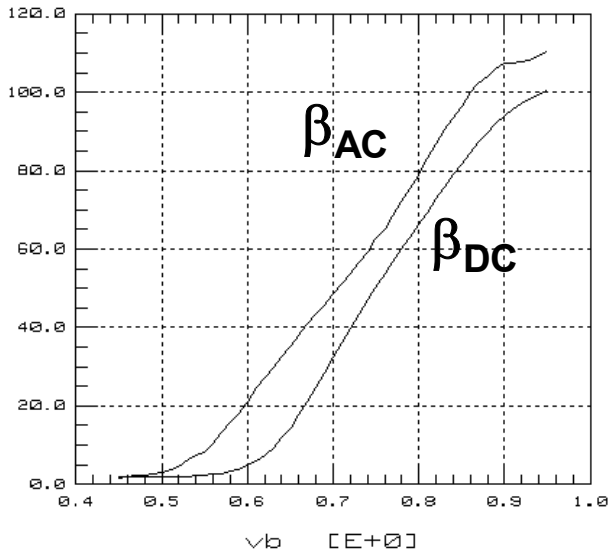

Figure 2.
Measured AC and DC current gain (β_{AC} and β_{DC}) the device from figure 2 above.

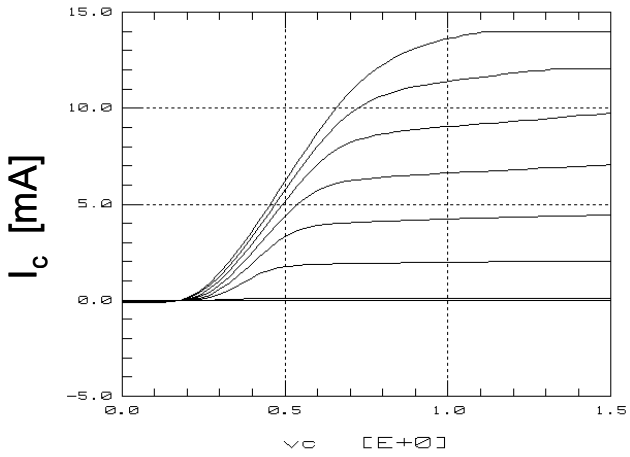

Figure 3.
Measured forward I_c-V_{ce} characteristics of the device from figure 2 above.

Figure 3 shows the forward Early characteristics of the $0.5x4\mu m^2$ DHBT device. Maximum current density in the devices was ~7 $mA/\mu m^2$. Breakdown (BV_{ceo}) on the SHBT transistors with 100nm collector was 3.1V. The current gain of the DHBT is somewhat lower but the breakdown is much higher at about 4.5V. The process produced HBT devices with f_t > 260 GHz on both DHBT and SHBT devices (V_{ce}= 1.5V, I_c ~ 10 mA) with drawn emitter area = $0.5x4\mu m^2$. Figures 4 and 5 plot the shows the f_t dependence on collector current for DHBT and SHBT devices, respectively. The f_t extrapolations in figures 4 and 5 are from single frequency measurement at 40 GHz assuming a -20dB/dec slope for each current bias point. Four values of collector emitter potential (V_{ce}) are shown in figures 4 and three in figure 5.

The new implanted subcollector devices are fully compatible with our standard IC process. [8] We have demonstrated very high yielding 31-stage CML ring oscillators containing about 100 transistors. The measured gate delay was as low as 7 psec with a power dissipation of < 6mW. Yield and uniformity of the oscillation frequency were as good as or better than results obtained on similarly prepared mesa etch wafers. To our knowledge, this is the first demonstration of cutoff frequency in excess of 260 GHz on patterned ion-implanted InP HBTs (both SHBT and DHBT devices) and the first demonstration of integrated circuits using such a process. [9,10]

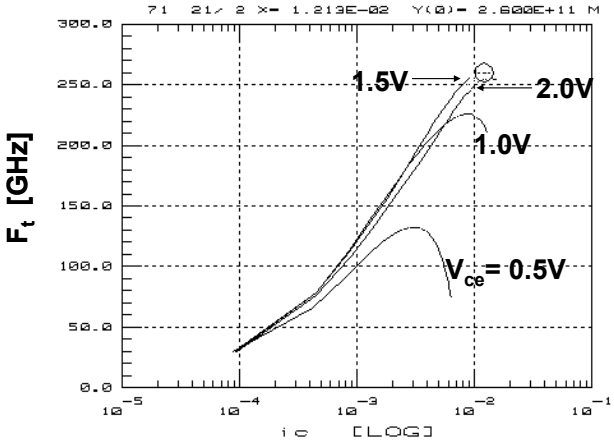

Figure 4.
Unity current gain (F_t) versus collector current for the DHBT device in figure 2 above.

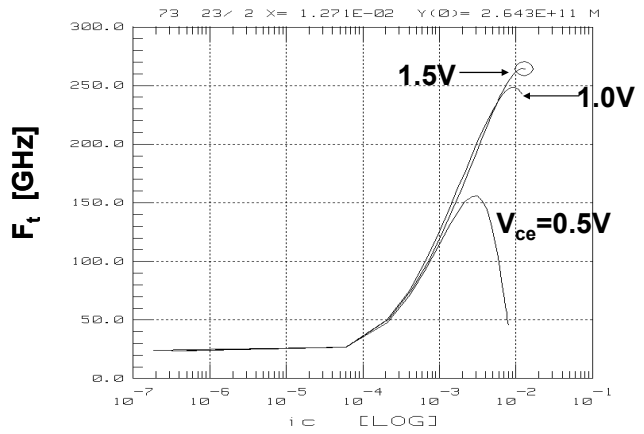

Figure 5.
F_t versus I_c for an SHBT device similar to the DHBT in figure 5 above in terms of layout, size, epi layer and metal thicknesses.

THERMAL RESISTANCE MEASUREMENTS

The promise of lowered thermal resistance has yet to be verified. In this paper we present measurements of the device thermal resistance from hotplate temperatures (T_{HP}) from 30 ^{o}C to 180 ^{o}C.

The method involves using the base-to-emitter voltage (V_{be}) at a constant emitter current density as a thermometer for sensing junction temperature. Thermal resistance was calculated following the approach outlined by Dawson. [4] Wafers were held on a heated stage using a vacuum hot-chuck with baseplate temperatures of 30, 60, 90, 120, 150, and 180^{o}C.

Devices were measured with an HP4142. High-temperature ground-signal-ground probes were used for device contact (Picoprobe model# 40A-GSG-150-P-HT). The base-to-emitter voltage (V_{be}) was swept over a 30mV range for 8 different collector-to-emitter bias voltages (V_{ce}). The range was chosen to include the values of V_{be} that produced the desired emitter current. The devices were evaluated at emitter current density (J_e) of 250μA/μm^2. The V_{ce} was swept from 0.6 to 2 V in 0.2 V steps and from 2 to 0.6 V in –0.2 V steps. The values of V_{be}, I_c, and I_b were recorded and averaged for each V_{ce} value. The emitter current (I_e) was calculated from Kirchhoff's Law. The power dissipated in the device is given by:

$$P_{diss} = (I_b \cdot V_{be}) + (I_c \cdot V_{ce}) \qquad [1]$$

Figure 6 compares the normalized values of R_{th} for SHBT, DHBT, and implanted subcollector DHBT devices all with emitter size equal to 0.5x2μm^2 measured at constant current density of 250 μA/μm^2. It can be seen that the thermal resistance of ~17 ^{o}C/mW was obtained for the SHBT device which compares well with previously published measurement on a similar sized device (1x1μm^2) with a slightly thicker collector. [11] The slight difference in values at higher temperatures is attributed to perimeter to area ratio effects as seen in previous measurements [11]. The larger perimeter-to-area ratio allows more heat to spread laterally reducing the junction temperature rise.

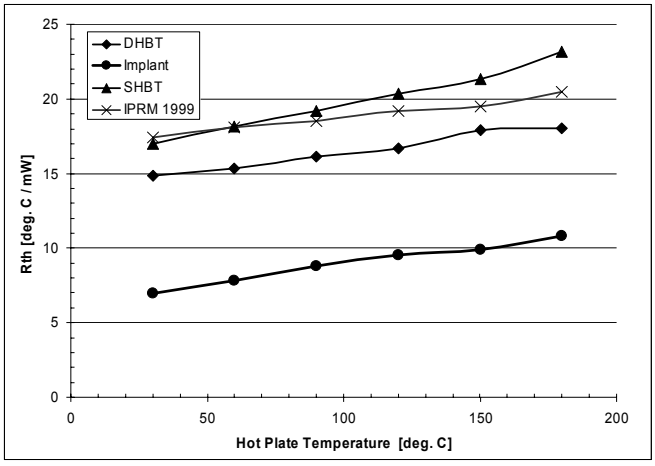

Figure 6.
Thermal Resistance of InP HBTs from 30 to 180 ^{o}C measured at a constant emitter current density of 250μA/μm^2.

The DHBT device from figure 6 shows a lower value of thermal resistance equal to 15 ^{o}C/mW compared to the SHBT device. This reduction in R_{th} is due to the replacement of the InGaAs collector layer in the SHBT device with InP collector for the DHBT. The reduction in Rth in the measured data here is less than previously reported for similar such InP HBT devices [12]. The devices measured in this report used a thinner InGaAs Collector material than previous reports. Since InGaAs is the material in the device stack with the lowest thermal conductivity, reducing the total InGaAs thickness will reduce R_{th}. Comparing SHBT with DHBT devices, the device pairs with the thicker InGaAs collectors are expected to display a greater difference in R_{th}.

The final curve in figure 6 plots the measured R_{th} for the $0.5x2\mu m^2$ DHBT device with the ion implanted subcollector was 7 ^{o}C/mW.

CONCLUSIONS

We have developed a device and IC process that makes use of selective ion implantation to define the subcollector contact layer of the HBT device. Following the patterned implantation, device layers were regrown on the implanted and annealed surfaces. These device layers are similar to those grown on InP substrates. This process has lead to the demonstration of both SHBT and DHBT devices with greater than 260 GHz. Further optimization of the base/subcollector overlap is currently underway to further improve the performance and yield of these deep submicron HBTs. [10]

We reported on the measured thermal resistance of these new ion implanted HBT devices. The measured values of R_{th} is greatly reduced in these HBT owing to the thermal shunting or spreading provided by imbedding the device subcollector in the InP substrate. In this process, the HBT is now surrounded by InP rather than the inter-layer dielectric materials which surround the device subcollector. Most ILD materials in use today have a lower thermal conductivity than InP. The reduced R_{th} allows the devices to operate a much lower temperature and therefore offer the potential to dramatically improve device lifetime.

ACKNOWLEDGEMENTS

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ACRONYMS

HBT: Hetero-junction Bipolar Transistor
TDMA: Time Division Multiple Access
J_e: Emitter current density
R_{th}: Thermal resistance
GSMBE: Gas Source Molecular Beam Epitaxy
TCAD: Technology Computer Aided Design
C_{jc}: Base-collector junction capacitance
MSI: Medium Scale Integration
ILD: Inter-Layer Dielectric
IC: Integrated Circuits
F_t: Unity Current Gain Cutoff Frequency