Observations of Current Blocking in InP/GaAsSb DHBTs

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KEYWORDS: HBT, InP, GaAsSb, Current Blocking

Abstract

Type II InP/GaAsSb transistors have attracted much interest in high speed microelectronics. However, Kirk-effect-induced current blocking was observed, limiting the highest achievable current density and hence the speed. In this work, we present an explanation as to the cause of current blocking in InP/GaAsSb DHBTs. The effects of collector thickness are investigated and methods to achieve higher current densities are proposed.

INTRODUCTION

GaAsSb is an attractive alternative material system to InGaAs for the base of HBTs due to a more favorable type II band line-up in the base-collector junction. The current blocking problem arising from the band discontinuity between the base and collector seen in type I DHBTs is eliminated due to the staggered type II heterojunction. In addition, type II transistors have a larger valence band discontinuity, providing superior hole blocking [1, 2]. Type II transistors do not see a bandgap spike in the base-collector junction, avoiding complicated bandgap engineering efforts that have plagued type I DHBTs [3]. With an all InP collector, type II InP/GaAsSb DHBTs are expected to have better thermal properties and a higher breakdown voltage when compared with type I InP/InGaAs SHBTs. InP/GaAsSb DHBTs have been reported to achieve f_T above 300 GHz, operating at current densities in excess of 450 kA/cm^2, with a BV_{CEO} greater than 6 V [4].

Despite the potential of InP/GaAsSb DHBTs, current blocking due to the base push-out effect under high current density was observed in our study and limits this material system in the pursuit of high speed transistors with reasonable breakdown voltages. In this paper, we report our investigation of the current blocking effect on InP/GaAsSb DHBTs. Our results showed that under high current injection, current blocking is observed, resulting in highly resistive I-V characteristics due to the shift in the quasi-fermi level under high current injection.

Current blocking phenomenon in type II DHBTs was investigated for a set of different collector designs with varying thickness as well as doping. A simple theory was used to explain the origin of this current blocking effect. Based on these results and observations, improvements in are proposed in layer structure design methodologies to achieve a higher performance.

LAYER STRUCTURE AND DEVICE FABRICATION

In this study, four different epitaxial structures were used. The layers were grown by MOCVD on semi-insulating, Fe doped, InP substrates. Wafer 1 consisted of a 150 nm InP collector, silicon doped to 3e16 cm^{-3} and a 30 nm $GaAs_{.51}Sb_{.49}$ base, carbon doped to 4e19 cm^{-3}. Wafer 2 consisted of an unintentionally doped 150 nm InP collector and a 25 nm $GaAs_{.55}Sb_{.45}$ strained base carbon doped to 6e19 cm^{-3}. Wafer 3 consisted of a 75 nm InP collector, silicon doped to 2e16 cm^{-3} and a 25 nm $GaAs_{.51}Sb_{.49}$ base, carbon doped to 7e19 cm^{-3}. Wafer 4 consisted of a 230 nm InP collector, silicon doped to 3e16 cm^{-3} and a 41 nm $GaAs_{.51}Sb_{.49}$ base, carbon doped to 5e19 cm^{-3}. The structures are summarized in Table 1. The devices were fabricated using a standard mesa process outlined in [5]. In the fabrication, a selective wet etching process was used in combination with electron beam lithography, for the emitter and the base, and optical lithograph for the collector. The intrinsic emitter and the base were connected by a microbridge.

TABLE 1
Summary of the layer structure for each wafer.

Wafer Num	Collector Thickness (nm)	Collector Doping (cm^{-3})	Base Thickness (nm)	Base Doping (cm^{-3})
1	150	3.00E+16	30	4.00E+19
2	150	uid (~1e16)	25	6.00E+19
3	75	2.00E+16	25	7.00E+19
4	230	3.00E+16	41	5.00E+19

RESULTS AND DISCUSSION:

The Gummel-Poon and the family of curves were measured for the four structures. Evidence of current blocking was seen in all four transistors. A typical curve is plotted as Fig. 1. At high currents, the device ceased to modulate and showed resistor-like output characteristics instead. This effect was not seen in InP/InGaAs SHBTs with a similar layer structure [6].

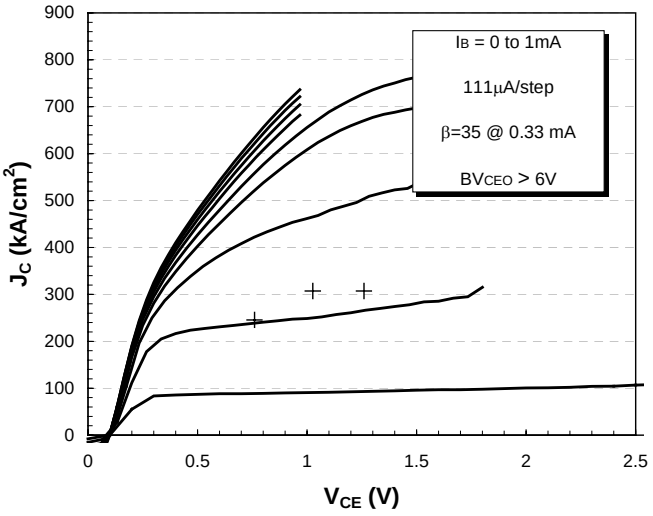


Fig 1: I-V curves for a 0.35 μm x 4 μm device on wafer 1.

The current density where the onset of current blocking occurs is best found from the Gummel-Poon plot (Fig. 2). The collector currents were normalized by the emitter area, and the base currents were not plotted for clarity. The plot shows that after a given current density, the collector current ceased to increase exponentially. The data also showed that current blocking in wafer 3 occured at the highest collector current density, J_c, followed by wafers 1, 2, and finally 4.

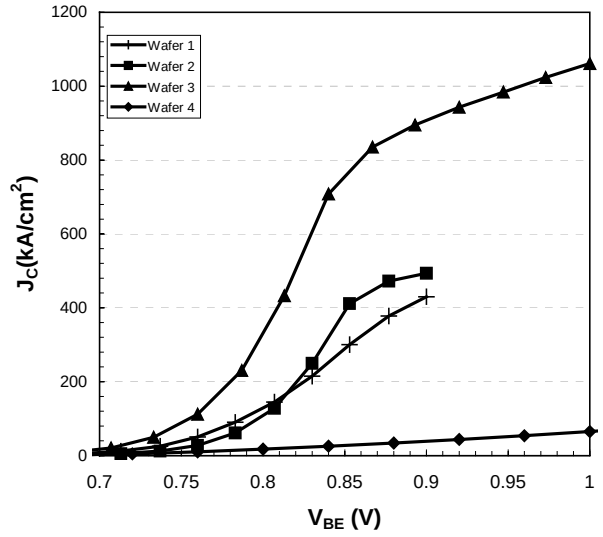


Fig 2: Gummel-Poon plot focusing on the high injection region. Under high injection, current increases linearly with voltage.

The current densites at the highest current gain are tabulated in Table 2 for a 0.8 μm x 12 μm on each of the structures. A direct comparison of wafers 1, 2, and 4 shows the effect the collector thickness has on J_c. The current density at which collector blocking occurred increased linearly as the collector thickness decreased. The slight offset of wafer 4 from the linear trend could be due to a slightly lower collector doping.

TABLE 2
DC current densities at which peak β is achieved for each collector design.

Wafer Num	Collector Thickness (nm)	Collector Doping (cm^{-3})	Max J_c (kA/cm^2) @ Peak β
1	150	3.00E+16	488
2	150	uid (~1e16)	411
3	75	2.00E+16	642
4	230	3.00E+16	177

To explain the appearance of current blocking in type II InP/GaAsSb DHBTs, we apply the Poisson's equation to the collector under high current densities. For an n-type collector, the 1-dimensional Poisson equation is reduced to equation 1, where E is the electric field, N_d is the doping, n is the injected electron density, q is the electron charge, and ε is the dielectric constant of the material.

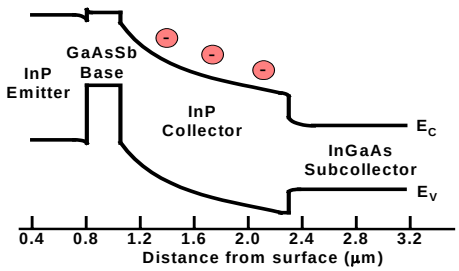
$$\frac{dE}{dx} = \frac{q}{\varepsilon} \bullet \left(N_d - n\right). \qquad (1)$$

For a low level injection HBT with an injected electron density <20% of the collector doping, the energy band diagram is shown in Fig. 3 (a). This figure was computed using the Model Solid Theory, which uses the deformation potential, the relation of the valence band to the vacuum level, and the bandgap to predict the band alignment at heterostructure interfaces [7]. For high level injection, the corresponding injected electron density increases, compensating the collector doping concentration, as indicated in Fig. 3 (b). When the electric field at the base-collector junction, E_{BC}, is sufficiently reduced, electron transport ceases to be primarily drift current. Due to the inability of the diffusion current to compensate for the reduction in drift current, the regions of low electric field behave as high resistance regions. We believe that these induced high resistance regions cause the current blocking observed in our DHBTs.

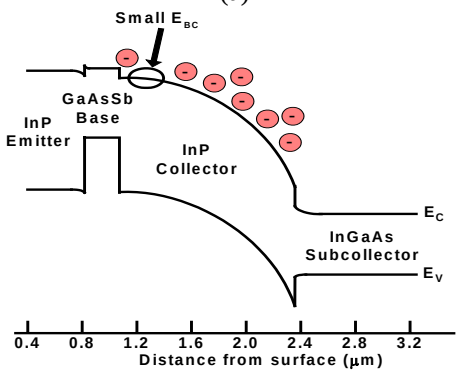
In order to estimate the value at which current blocking will occur, the Poisson's equation was solved for the current density at E_{BC}=0 V/cm to yield:

$$J_B = v_{sat}\left(q \bullet N_C + \frac{2 \bullet \varepsilon_C * \left(V_{BC} + V_{BI}\right)}{W_C{}^2} \right). \qquad (2)$$

For a 1500 nm, InP collector, doped at 3e16 cm^{-3}, a saturation velocity of 1.5e17 cm/s, a built-in potential of 0.65 V, typical for a n- InP/p+ GaAsSb junction, and a V_{BC} of 0.5 V, the current density required for E_{BC}=0 V/cm is 242 kA/cm^2.



(a)



(b)

Fig. 3: (a) Band diagram for a 150nm InP collector, Silicon doped to 3e16 cm^{-3} and a 30nm $GaAs_{.51}Sb_{.49}$ base, Carbon doped to 4e19 cm^{-3}, (b) for high level injection (>250 kA/cm^3).

There are a number of simplifications in this model. First, the velocity the electron gains from being ballistically launched from the base is ignored. Current spreading and that the electron velocities vary with the electric field are also neglected. However, even with these simplifications, the derivation can be used to predict a number of trends, such as the effect the collector thickness has on J_B.

While the effects of the emitter thickness is demonstrated, the effects of strain and the doping could not be seen in this study. For a 150 nm collector, a 1e16 cm^{-3} change in collector doping would require a change of 24 kA/cm^2 to provide compensation. Similarly, the strain from changing the base composition to $GaAs_{.55}Sb_{.45}$ will change the built-in potential between the base and the collector by approximately 0.05 eV, as calculated by the model solid theory. This necessitates an increase in J_B of approximately 7 kA/cm^2. In both cases, such a small change in J_B could not be distinguished from process variations.

The built-in potential at the base-collector interface offers some insight as to why the current blocking is more severe in type II DHBTs than other HBT structures. If the Fermi levels of the base and the collector are assumed to be at the edge of the valence band and the conduction band respectively, the built-in potential of an InP/GaAsSb DHBT is 0.7 eV. In contrast, the built-in potential of an InP/InGaAs DHBT is 1 eV. The increase in the built-in potential results in a stronger field at the base-collector junction, retarding the current blocking effects.

The peak performance was observed for a 0.5 x 16 μm^2 transistor from wafer 1 with an f_T of 228 GHz and an f_{MAX} of 155 GHz. The peak f_T of this device occured at a current density of 388 kA/cm^2, corresponding to a current of 31 mA. Both the peak f_T and the corresponding current density were significantly lower than those reported for InP/InGaAs SHBTs with similar layer structures. The corresponding InP/InGaAs SHBT had an f_T = 382 GHz and f_{MAX} = 250 GHz obtained at 511 kA/cm^2 [6].

Fig. 4 shows a plot of f_T as a function of J_c for devices biased at a fixed V_{BC} with varying V_{CE} for wafer 1. The peak f_T occured at V_{CE} = 1.26 V (V_{BC} = 0.5 V, J_c = 388 kA/cm^2); beyond this, the performance decreased due to current blocking. Additionally, points for which peak f_T was obtained are plotted for different V_{CE} in Fig. 1. The peak f_T was obtained near the peak β for the particular bias.

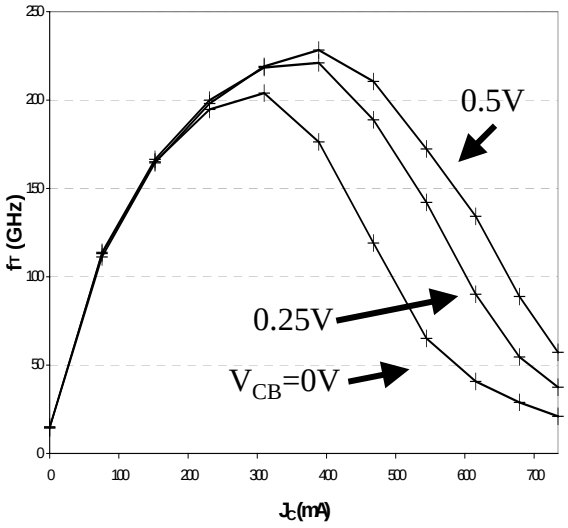


Fig 4: f_T vs collector current for different V_{BC} bias points.

Methods for overcoming the blocking effects are to engineer the collector layer to increase E_{BC} or reduce the effect the injected current has on E_{BC}. Increasing the collector doping will reduce the effect the injected current has on E_{BC}. Reducing the collector thickness or adding strain to the base layer will increase E_{BC}. Any of these methods will retard the onset of current blocking, increasing the associated high frequency performance.

CONCLUSION

We have fabricated different collector structures for type II DHBTs and have observed their effects on current blocking. With a simple calculation using the conventional Poisson's equation, this phenomenon is readily explained

and understood. Our current results show that the onset of current blocking scales linearly with collector thickness. Additionally, we believe that further improvement can be achieved through an increase in the collector doping or increasing the built-in potential at the base-collector junction.

ACKNOWLEDGEMENTS

The authors would like to thank the University of Texas, Austin for growing wafer 3, Microlink for growing wafer 4, Richard Chan and Dr. David Caruth for their valued technical discussions, Mr. Frank Stolli from BAE systems for the DARPA-TFAST program management support, DARPA-TFAST program manager Dr. John C. Zolper, and ARL contact manager Dr. Alfred Hung for program support.

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ACRONYMS

f_T: Cutoff frequency
BV_{CEO}: Breakdown Voltage, Collector-Emitter Junction, With Base Open
HBT: Heterojunction Bipolar Transistor
MOCVD: Metal Organic Chemical Vapor Deposition
SHBT: Single Heterojunction Bipolar Transistor
DHBT: Double Heterojunction Bipolar Transistor
SI: Semi-Insulating