C_{bc} Reduction in Si-implanted Subcollector HBTs

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Abstract

We demonstrate the first small area emitter (1.4 × 3 μm^2) N-p-n AlGaAs/GaAs HBTs fabricated with N^+-implanted subcollectors in a high volume manufacturing environment. The subcollector region was defined by multiple N^+ implants of various doses and energies on a semi-insulating GaAs substrate, and the remaining HBT layers were grown by MOCVD. To evaluate the impacts of C_{bc} reduction, devices with varying subcollector areas were fabricated for comparison. Small signal s-parameter data was measured to extract f_T, f_{max} and C_{bc}. By varying the implanted subcollector area, the base-collector capacitance C_{bc} was reduced by almost 40% using this manufacturable process. The common emitter current gain of devices fabricated by this implant/epitaxial hybrid process is about 50 which is similar to our baseline device, indicating good material quality using this technique.

Introduction

III-V-based heterojunction bipolar transistors (HBTs) have attracted great attention due of their excellent switching speed and current driving capability. Many impressive high-speed digital, analog, mixed signal, power amplifier circuits, including commercially successful products, have been demonstrated using HBTs [1]-[3]. To further improve the device performance and scaling in these applications, the reduction of the extrinsic base-collector capacitance of HBTs is essential. Several research groups have demonstrated C_{bc} reduction and improved f_{max} by regrowth on patterned subcollectors [4], deep ion implants through the external base layer [5], or by removing the extrinsic sub-collector altogether [6, 7]. However, these methods all have drawbacks with respect to manufacturing. Regrowth on patterned subcollectors results in increased topology, which limits the integration level, as well as increased costs (two growth cycles). Deep implants tend to damage the base layer, resulting in increased base resistance. Although partial/complete removal of the subcollector can achieve excellent RF performance, it may result in poor manufacturing yield as well as complicating thermal management issues. An alternate approach is to define subcollector areas by selective area N^+-implants and then grow the remaining layers [8, 9]. This is very similar to the approach used to build silicon bipolar transistors. However, due to the low activation efficiency of high dose n-type implants in GaAs substrates and the quality of materials grown on implant-damaged surfaces [10, 11], this approach has never been realized in any small area emitter N-p-n type of GaAs-based HBTs.

In this paper, we report the first demonstration of small area emitter (4.2 μm^2) N-p-n AlGaAs/GaAs HBT fabricated with N^+-implanted subcollectors. We have previously reported DC results of large area (72 × 72 μm^2 emitter) devices and demonstrated that high quality MOCVD material could be grown on substrates with blanket N^+ implants [12]. In this work, we adopted a similar N^+ implant process as reported in [12]. The subcollector regions were defined by multiple Si^+ and Se^+ implants on a semi-insulating GaAs substrate and devices with varying extrinsic base-subcollector areas were fabricated for C_{bc} comparison. The common emitter current gains of devices fabricated by this implant/epitaxial hybrid process are about 50. This value is comparable to our baseline HBTs, again indicating good material quality. Small signal s-parameter data was measured to extract f_T, f_{max} and C_{bc}. At a collector current density of 5 × 10^4 A/cm^2, f_T and f_{max} of 57 and 85 GHz were obtained, respectively for the device with the smallest subcollector dimensions. This data indicates a reduction in total C_{bc} of almost 40% with a corresponding f_{max} improvement of more than 35% compared to the baseline device.

Device Fabrication

The starting substrates were standard 4-inch epi-ready semi-insulating GaAs wafers with orientation 2° off (100) towards <110>. This is the standard for production MOCVD growth. Before the subcollector patterning and N^+ implantation, the wafers were encapsulated with 40 nm of reactively sputtered silicon nitride (Si_3N_4). After implantation and photoresist removal, high temperature anneals for post-implant activation was performed at 950°C for 6 minutes by using a rapid thermal annealing process (RTP). A very high quality Si_3N_4 thin film is required because of the annealing temperature. After this activation anneal, the silicon nitride was removed and the HBT

structure was completed by the sequential MOCVD growth. A commercial vendor provided the MOCVD growth. The transistors were then fabricated using a standard Rockwell's HBT process [1]. Ti/Pt/Au metal was deposited to form the base contact. A wet etch was used to etch through the collector and expose the implanted sub-collector. AuGe/Ni/Au was used for the collector and emitter contacts. The sample was alloyed in a RTP system for 2 minutes at 390°C. As can be seen in Figure 1, a low sheet resistivity of 13 Ω/□ can be achieved by Si and Se co-implantation. This resistivity is comparable to an epitaxial layer with thickness 600 nm doped to $5x10^{18}$ cm^{-3} and is adequate for device and circuit applications.

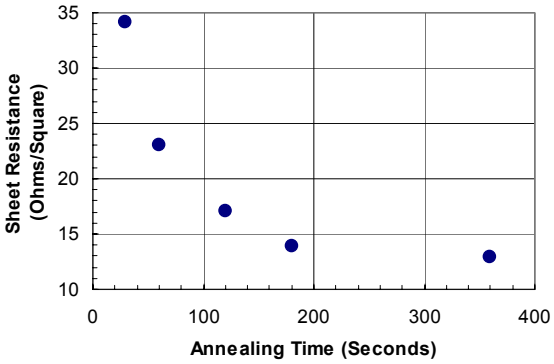

Figure 1: Sheet resistance verses annealing time for a Si and Se co-implanted GaAs wafer annealed at 950°C with a sputtered Si_3N_4 thin film

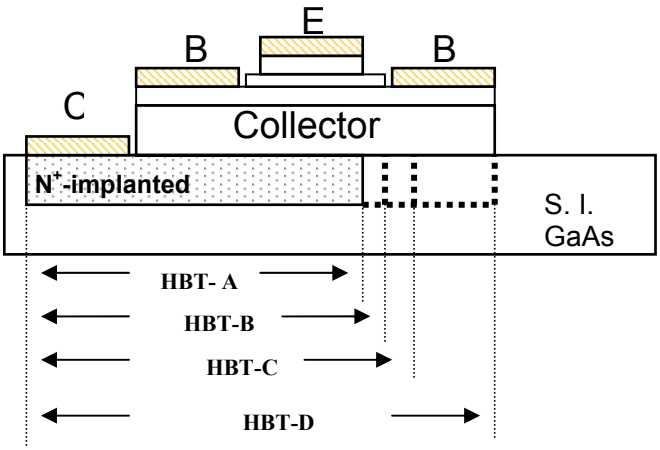

Figure 2: A schematic cross section of the proposed HBTs: HBT-A, HBT-B, HBT-C and HBT-D.

In order to evaluate the impact of reduced extrinsic C_{bc} on the device performance, devices with various subcollector sizes were layed out on the mask set. A schematic cross section of the fabricated HBTs with four different layouts is shown in Figure 2. If we neglect the straggling effect of implantation and process misalignments, under the emitter and base contacts HBT-A, HBT-B, HBT-C and HBT-D represent devices with N^+ implant layout areas of 9, 10.92, 13.74, 28 μm^2, respectively.

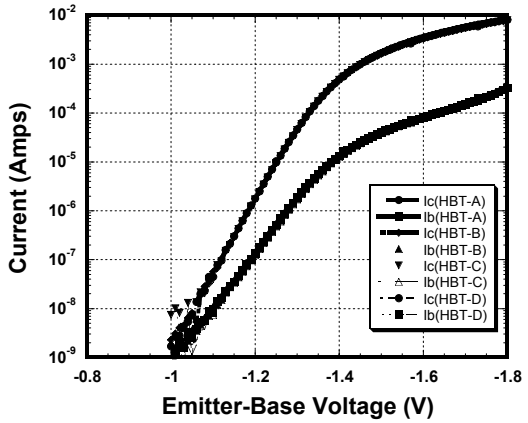

Figure 3: The Gummel plots of small area emitter (1.4 × 3 μm^2) HBT-A, HBT-B, HBT-C and HBT-D.

Results and Discussion

It is desirable to have low sheet and contact resistances for the implanted layer because collector resistance can have a substantial impact on device scaling and on the maximum attainable output voltage swing. Using this implant process, a sheet resistivity of 13.5 Ω/square is obtained, which is consistent with our previous report [12], and collector specific contact resistance of mid 10^{-7} Ω–cm^2 as determined by transmission line measurements (TLM). These results are comparable to epitaxially grown subcollectors and are adequate for device and circuit applications. The Gummel plots of the fabricated devices: HBT-A, HBT-B, HBT-C and HBT-D are shown in Figure 3. All four transistors show very similar DC characteristics, indicating little device degradation caused by the varying subcollector areas. In order to evaluate the impact on the C_{bc} reduction in four different layouts, small signal s-parameter measurements were performed to extract device f_T, f_{max} and the C_{bc}. At V_{CE} = 1.5 V and J_C = 5 × 10^4 A/cm^2, the HBT-A with emitter area of 4.2 μm^2 and

the smallest subcollector area exhibited f_T of 57 GHz and f_{max} of 85 GHz, as shown in Figure 4.

Comparing the results for HBT-A to those of HBT-D, which emulated our baseline HBT with emitter area of 4.2 μm^2 and a standard subcollector area, we observe that the f_T and f_{max} increased by 7 GHz (14%) and 23 GHz (37%), respectively. The values of C_{bc} (at V_{CE} = 1.5 V and J_C = 5 × 10^4 A/cm^2) were extracted following the method proposed by Pehlke [13]. Figure 5 shows the extracted C_{bc} versus implanted subcollector areas and corresponding f_T and f_{max}. As shown in the figure, the C_{bc} decreased with decreasing the subcollector areas and both f_T and f_{max} increased accordingly-as expected. A 38% reduction (from 19.8 fF to 12.3 fF) in C_{bc} has been achieved using this manufacturable process.

To first order the C_{bc} should have a close to linear relation with the subcollector area and the reduction of C_{bc} should be greater than 38 %. However, there are several possible causes for this discrepancy. The mostly likely cause is due to the lateral straggling effect during N^+ ion implantation. Therefore, the effective subcollector areas were actually bigger than the designed layout areas. The lateral straggling in our process was estimated to be around 0.7 to 0.8 μm based on the extracted data, which was almost a one to one ratio to our projected implant depth calculated by a Monte-Carlo TRIM program [14]. This straggle, and its shape, will impact the peripheral component of the C_{bc}, in addition to the area dependent C_{bc}. It should also be noted that we are removing extrinsic Cbc from the device – this should allow for a greater capacitance cancellation effect as more of the device becomes intrinsic [15]. We believe the device performance can be further improved by including the straggling effect and minimizing periphery in future layout designs. A more than 70 % reduction in C_{bc} can be expected.

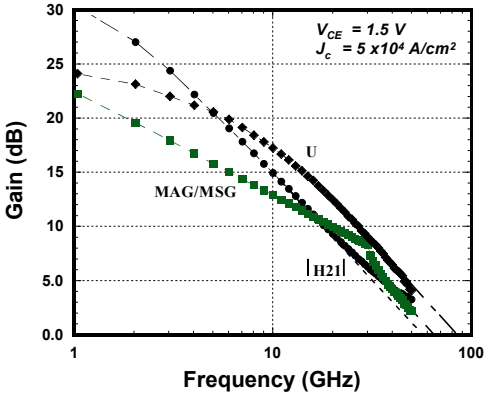

Figure 4: The measured $|H21|$, MAG/MSG, and U versus frequency of HBT-A at V_{CE} = 1.5 V and J_C = 5 × 10^4 A/cm^2

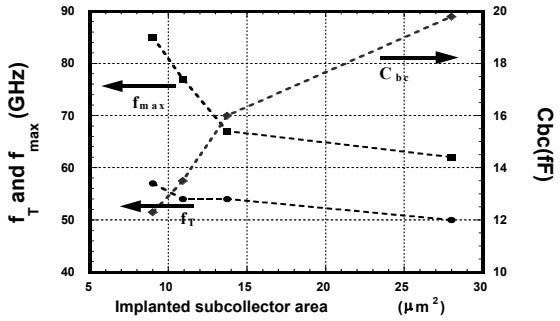

Figure 5: f_T, f_{max} and extracted C_{bc} versus implanted subcollector area at V_{CE} = 1.5 V and J_C = 5 × 10^4 A/cm^2.

Summary

In summary, we have demonstrated the first small area emitter N-p-n AlGaAs/GaAs HBTs using N^+-implanted subcollectors in a high volume GaAs manufacturing line. A 38% reduction in C_{bc} and a corresponding 37% increase in f_{max} have been achieved. With this technique, C_{bc} can be significantly reduced allowing better scaling and power performance for III-V HBTs.

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