

High Performance GaN HEMTs on 3-inch SI-SiC Substrates

K.S. Boutros, M. Regan, P. Rowell, D. Gotthold,* and B. Brar
Rockwell Scientific Company
1049 Camino Dos Rios, Thousand Oaks, CA 93021
805-373-4104; fax: 805-373-4860; e-mail: kboutros@rWSC.com
*Emcore Corp. Somerset, NJ.

INTRODUCTION

Gallium Nitride (GaN) HEMTs are the focus of intense research and development due to their potential for the realization of MMIC power amplifiers (PAs) with high gain and record levels of power delivery [1]. Much of the work in GaN HEMT development has been concentrated on performance demonstration on 2" SiC and Sapphire substrates. Multiple groups have demonstrated GaN HEMTs delivering record power performance at microwave and mmWave frequencies [2,3]. Recently, there has also been major progress in the improvement of uniformity and reproducibility of GaN HEMT 2" epitaxial wafers on both substrates, available through multiple electronic material foundries [4,5]. Of the two substrates, SiC offers a better thermal conductivity and lower dislocations in the GaN film, which has a large impact on the performance of GaN power devices. However, until recently, only 2" SI-SiC was available for GaN HEMT development. Scaling of the GaN technology to 3" will result in doubling the number of MMIC die per wafer. This will be instrumental in the reduction of the overall cost of GaN-based MMICs, and ultimately, in the introduction of this technology into commercial and military systems.

This paper presents the successful scaling of GaN HEMT fabrication process to 3" semi-insulation (SI) SiC substrates using 0.18 μm gate-length technology. A base-line GaN fabrication process, suitable for mmWave applications, is demonstrated on 3" GaN epi-wafers. GaN HEMTs were fabricated with high yield and uniformity. Device performance on 3" substrates was similar to what can be achieved on material grown on 2" SiC. The basic device fabrication technology, along with DC and RF characteristics of GaN HEMTs fabricated with 0.18 μm technology are presented. [Keywords: GaN HEMTs, wafer scaling, 3-inch SI-SiC substrates, mmWave power MMICs.]

EXPERIMENTAL

The epitaxial layers consist of an AlGaIn/GaN, non-intentionally doped π -HEMT structure [6]. The GaN epi is grown on 3" semi-insulating 4H-SiC by metal-organic chemical vapor deposition (MOCVD) in a commercial, multi-wafer reactor. Scaling to 3" SiC substrates was accomplished by transferring a known growth recipe from 2" reactors to the larger 3" reactor. The material was characterized with contact-less sheet resistance mapping and showed an average sheet resistance of 400 Ω/sq with a one-sigma uniformity of approximately 5%, indicating a high quality and uniformity of the 2-DEG. The devices were fabricated in our high yield, baseline High-Power Amplifier process, which was developed on 2" GaN epitaxial wafers with a reproducible yield of 85% on 2-finger 200 μm wide devices. Stepper lithography is used to define the multiple process layers, and e-beam lithography is used to define the 0.18 μm gates. The source and drain contacts are based on a proprietary refractory-metal process, which results in sharp edge definition and smooth surface after contact alloy. Typical contact resistance using our process is less than 1 $\Omega\text{-mm}$. A Si_3N_4 passivation layer was used

to suppress the RF dispersion. Device isolation is achieved using implant isolation, and two-level interconnect with air-bridge technology is used to complete the device fabrication process.

Device testing is performed on-wafer using automated test equipment. A probe-card is used for DC PCM-device testing and TLM measurements, while coplanar probes are used for RF measurements. Various DC parameters are extracted and mapped across the 3" wafers, including input, output, and sub-threshold characteristics, and sheet and contact resistances of the epi-layers. Small signal S-parameters up to 50 GHz are also extracted and used to calculate f_t and f_{max} of the devices. Average values and variances of device parameters are extracted and plotted using a software program to determine yield and correlation trends across the 3" wafers.

RESULTS AND DISCUSSION

Results from two 3" wafers are presented in this paper. TLM measurements on the completed wafers show an average sheet resistance of 407, and 466 Ω/sq , consistent with the contact-less sheet resistance results obtained prior to processing. Typical contact resistance value of 0.8 $\Omega\text{-mm}$ was obtained, indicating good contact quality on the 3" epitaxial films. Mapped DC device characteristics on single-finger, 40 μm devices show a saturation current $I_{\text{dss}} \sim 760$ mA/mm, an extrinsic transconductance $g_{\text{m,max}} \sim 270$ mS/mm, and $V_{\text{th}} \sim -5\text{V}$, with one-sigma uniformities better than 10%. PCM device yield was approximately 80% across the 3" wafer, with most of the yield loss occurring on edge-fields. RF device data was generated on coplanar 2-finger devices with 200 μm gate-width. An average f_t of ~ 70 GHz and an f_{max} of ~ 120 GHz were measured across the 3" wafer. A similar uniformity of 10% in RF device performance is observed. These results show that the GaN process has been successfully scaled to 3" substrates while maintaining the same device performance obtained on 2" substrates with similar device epi-layer structures. Additionally, maintaining high yield in the 3" process indicates that overall cost reduction can be accomplished by going to a larger diameter substrate.

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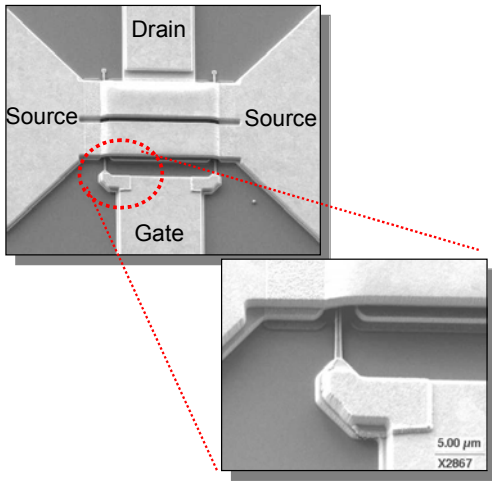


Figure 1. SEM image of the baseline two-finger GaN device showing the T-gate topology, multi-level metallization and interconnect using air-bridge technology.

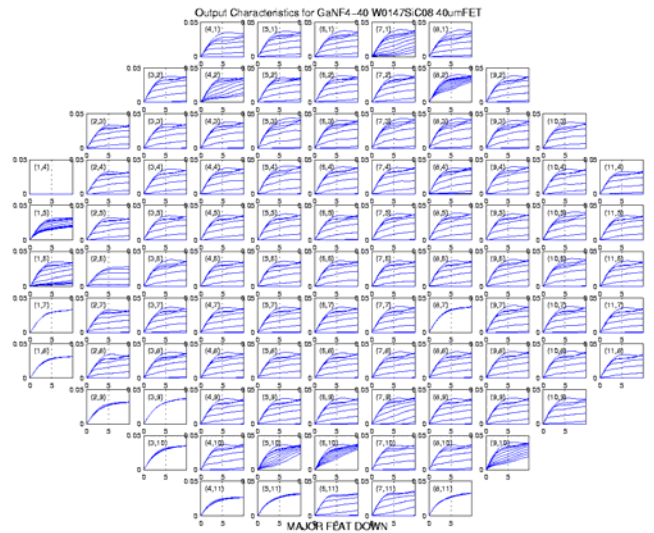


Figure 4. Output characteristics map of 40 μm PCM devices across a 3" GaN wafer. A total of 97 fields are measured, showing a device yield of 82% and high uniformity.

Wafer #	W0190SiC03		W0147SiC08	
	Value	σ (%)	Value	σ (%)
TLM Rsh (Ohm/sq.)	407	6.3	466	3.3
I_{dss} (mA/mm)	794	5.1	764	5.2
Gmmax (mS/mm)	264	5.9	273	8.3
F_t (GHz)	74.9	5.0	72.7	7.5
F_{max} (GHz)	125	3.7	119	7.8

Figure 2. Summary of average DC and RF performance on two 3" GaN HEMT wafers. A one-sigma uniformity of better than 10% is observed on both wafers.

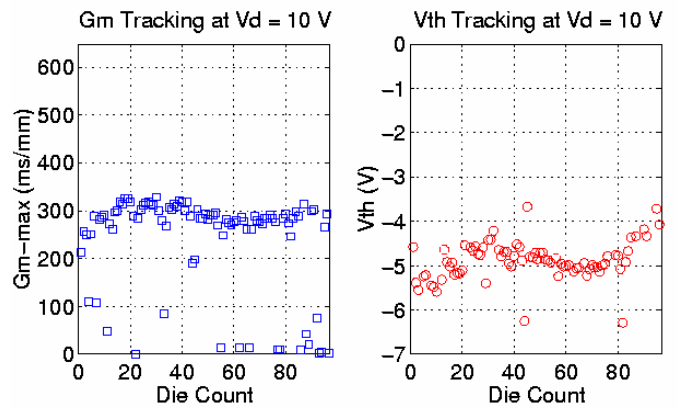


Figure 4. Transconductance and threshold voltage tracking across a 3" GaN wafer, showing a very narrow data spread across the wafer.

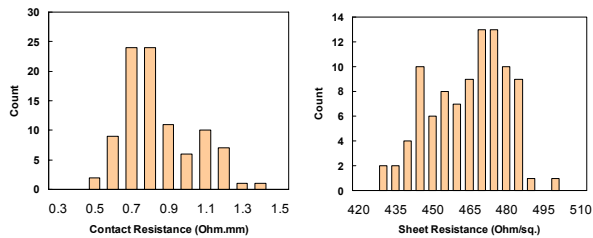


Figure 3. Histogram of TLM measurement results. 97 fields are measured across the 3" wafer. An average $R_c = 0.8 \Omega \cdot \text{mm}$, and average $R_{\text{sheet}} = 466 \Omega/\text{sq}$ are obtained.

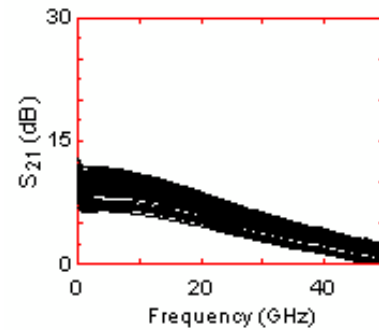


Figure 5. S_{21} spread on 2-finger 200 μm -wide devices across a 3" GaN HEMT wafer. The variation in f_c and f_{max} across the wafer shows a one-sigma uniformity better than 10%.