GaN HFET digital circuit technology

Tahir Hussain, Miroslav Micovic, Tom Tsen, Michael Delaney, David Chow, Adele Schmitz, Paul Hashimoto, Danny Wong, J. S. Moon, Ming Hu, Janna Duvall, Doug McLaughlin

HRL Laboratories, LLC, 3011 Malibu Canyon Road, Malibu CA 90265
email:thussain@hrl.com

Keywords: GaN HFET, Harsh Environments, Control Electronics

Abstract:

We report on a demonstration of GaN digital circuits implemented in a first generation GaN digital technology, which has yielded circuits of considerable complexity. We have implemented simple logic blocks, comparators, ring-oscillators and frequency dividers. We have yielded a 31-stage ring-oscillator using 217 transistors [1]. As a result of unique material characteristics GaN digital control circuits have the potential to operate in high radiation environments, at elevated temperature, and directly from high voltage rails. While we have successfully operated 31-stage GaN ring-oscillators at 265C, we believe that these circuits can operate at significantly higher temperatures and will be tolerant of total dose radiation exposure.

INTRODUCTION

Heterostructure Field Effect Transistors based on the GaN/AlGaN material system (GaN HFET) have been extensively studied in recent years. The overriding interest has been in power applications at X-band and higher frequency bands [2]. There has also been some interest in low noise applications where the robust nature of the GaN HFET makes it attractive [3]. We have recently reported a successful implementation of GaN digital circuits. The same material properties of the GaN/AlGaN heterostructure that make it attractive for the power and robust low-noise applications, namely the wide band-gap, high breakdown field and high saturation velocity, make it suitable for digital control applications in harsh environments. These applications include, but are not limited to, control electronics for aircraft and automobile engines, commercial well-logging, nuclear reactors, and spacecraft.

EXPERIMENT

A robust, high yield process with good uniformity is required for fabrication of digital circuits of moderate or even low complexity. The material growth and GaN HFET fabrication process is substantially similar to previously published work [4] and only repeated here in summary. To our knowledge, HRL is the only laboratory to have reported on a process suitable for fabrication of GaN digital circuits. Epitaxial structures for fabrication of GaN circuits were grown by plasma assisted MBE. The AlGaN/GaN HFET device structure was deposited on a semi-insulating SiC substrate and utilizes a heavily n+ doped GaN cap layer to facilitate fabrication of ohmic contacts. Device threshold voltage was adjusted using gate-recess etching. The device fabrication process features 4μm source-drain separation, 1-μm-long optical gates, SiN passivation and two levels of metallization. Varying gate periphery was utilized to implement different circuit functions, with the smallest device being 3μm wide. The gate to drain spacing has an effect on the breakdown voltage of the device, and can be adjusted for high voltage operation. As the GaN/AlGaN HFET is a depletion mode device, Schottky diodes were used for voltage level shifting required to implement complementary logic functions.

Figure 1 shows a micrograph of a comparator circuit corresponding to the schematic diagram shown in Fig.2. The circuit is configured as a differential pair. Pull-up loads are made of two FETs in series. The lower FET is several times larger than the upper one such that the output resistance of the combined configuration is higher than a single GaN FET load. Cascoding is used to increase the output resistance of switching FETs in an attempt to increase circuit DC gain, which is relatively low in such high voltage applications.

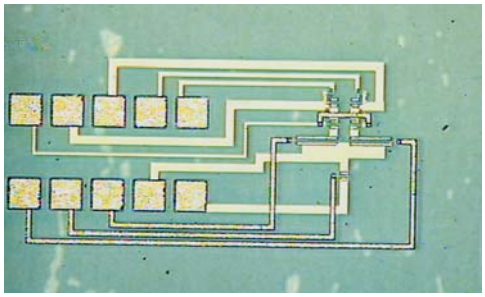

Figure 1 Micrograph of a GaN HFET comparator circuit.

A transfer curve of the comparator circuit is shown in Fig.3 for reference voltage Vref=-1.5V, Vdd is 20V and casc=7V. Here the input voltage b1 is compared to b0=2V, and measurements at complementary outputs z0 and z1 are shown. The solid curves are simulated and the broken curves are for measured data. Resolution of the comparator is seen to be better than 0.2V. Referring to the inset of Fig.3, with input resolution down to

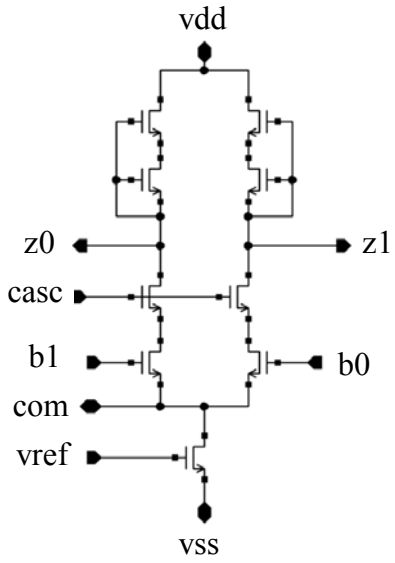

Figure 2 Schematic diagram of the comparator circuit.

20mV, we believe the resolution of the circuit is actually about 50mV.

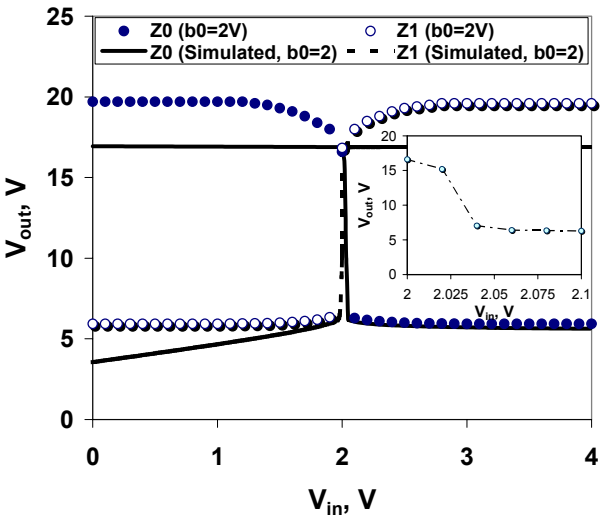

Figure 3 Measured and simulated transfer curves of the GaN comparator circuits.

We adopted a MOSFET model (LEVEL=1) for GaN HFET devices in this circuit design. Due to a crude set of model parameters used for model benchmarking, SPICE simulations do not perfectly match measured data. Although the rough model seems to cause discrepancies between the simulated and measured DC high level voltages, one important measure of a comparator design, its resolution, turns out to be fairly consistent at about 50mV. Output low is also measured to be close to what is simulated.

A 31-stage ring oscillator was constructed using thirty-one copies of buffered FET logic inverters and one

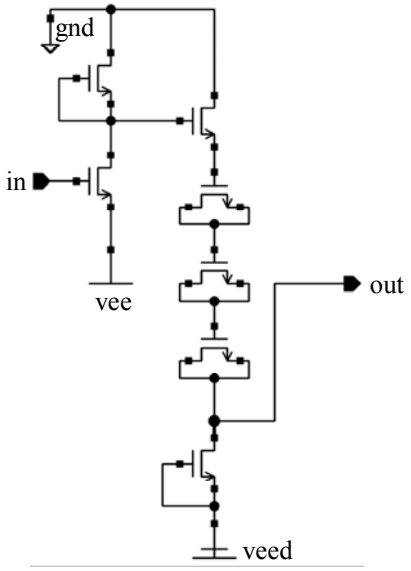

Figure 4 Schematic diagram of the inverter block used in the 31-stage ring oscillator.

output driver. Figure 4 shows a schematic diagram of the inverter block, which consisted of an inversion stage and a source follower with three diode-level shifts. Such a logic gate has been commonly used in compound semiconductor depletion mode FET logic circuit design for its high noise margin and high current drive capability. The GaN HFET devices have a typical threshold voltage of -4 volts, which mandated a level shifting stage in each logic gate. Each gate-to-source/drain Schottky diode in this technology has a barrier height of ~1.4 volts. Two negative power supplies are used, -6 volts for the inversion stage and -12 volts for the source follower. The output driver is included to drive a 50-ohm load from ground.

The frequency and time domain outputs of the ring-oscillator are shown in Figure 5. The 93.6MHz

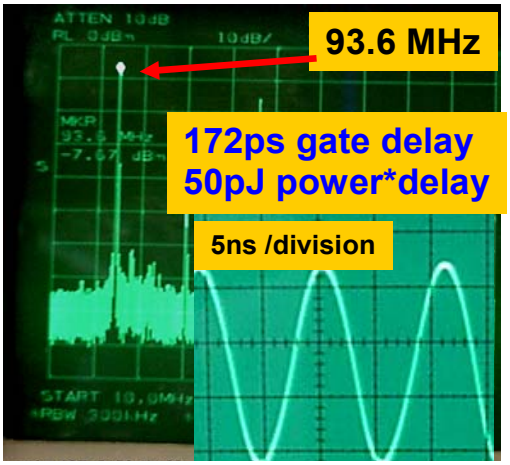

Figure 5 Frequency and time domain output of the 31-stage ring oscillator.

oscillation frequency corresponds to a 172ps per stage delay and a power-delay product of ~50pJ. Figure 6 shows the performance of the 31-stage ring-oscillator as a function of base-plate temperature. Although the per-

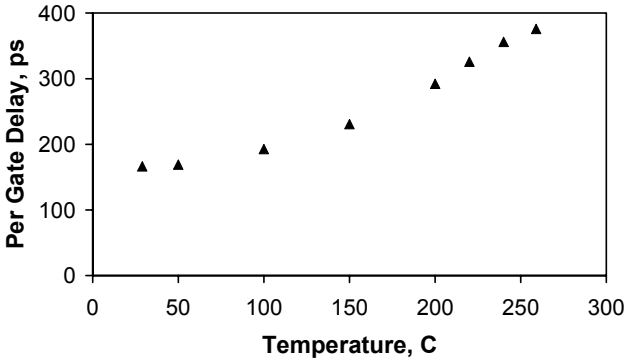

Figure 6 Plot of per-gate delay as a function of base plate temperature.

gate delay of the circuit increases with increasing base-plate temperature, the circuit is fully functional and the original performance is recovered upon returning the base-plate to room temperature.

CONCLUSIONS

A technology for digital control circuits with potential to operate in harsh environments was developed. Working circuits of modest complexity including voltage comparators and ring-oscillators were yielded. The ring-oscillator performance was measured to a temperature of 265C and it was found to revert to original performance after returning to room temperature.

REFERENCES

[1] T. Hussain et al., "GaN HFET Digital Circuit Technology for Harsh Environments" IEE Electronics Letters, Vol. 39, #24, pp 1078-79, Nov. 2003

[2] M. Micovic et al., 'K-band GaN power HFETs with 6.6 W/mm CW saturated output power density and 35% power added efficiency at 20 GHz' Device Research Conference, 2001, 25-27 pp 199 –200, June 2001

[3] T. Hussain et al., 'GaN HFETs with excellent low noise performance at low power levels through the use of thin AlGaN Schottky barrier layer' IEDM 2001 Technical Digest., pp 25.3.1 -25.3.4

[4] M. Micovic et al., 'AlGaN/GaN heterojunction field effect transistors grown by nitrogen plasma assisted molecular beam epitaxy' IEEE Transactions on Electron Devices, Volume: 48 (3), pp 591 –596, March 2001

ACRONYMS

HFET: Heterostructure Field Effect Transistor

GaN/AlGaN:Gallium Nitride/Aluminum Gallium Nitride