Sub 100nm T-Gate Uniformity in InP HEMT Technology

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Abstract

This work describes the improved uniformity of short gate length (sub100nm) T-gate lithography observed for InP HEMT devices through the development of a non-annealed ohmic contact process. The incorporation of such a process allows the reversal of ohmic and gate levels as part of a standard device process flow. This eliminates fluctuations in the gate geometry that result from the spinning of gate resists across a non-planar surface i.e. between the source and drain contacts.

INTRODUCTION

With the development and implementation of various sub 100nm gate length processes into III-V and specifically InP HEMT technologies, extremely high device performance figures of merit have been reported [1]. However, the yield and uniformity of such devices is often affected by the extreme lithography steps required for their realisation. In particular, the consistency of producing sub 100nm T-gates of a desired gate length can be challenging as subtle variations in the device processing which are not apparent for longer gate length devices play a larger role at these reduced dimensions. One example of this includes the effect of resist thickness fluctuations that can occur when spun over a non-planar surface i.e. between source and drain ohmic contacts within a HEMT fabrication process. These fluctuations will depend on various factors, including the resist strategy, the height of the ohmic metallisation and separation of the contacts. The T-gate profile as defined by electron beam lithography between the ohmic contacts will then depend upon the distribution of resist between them. Often this results in non-uniformity of the gate dimensions along the width of the device and in the extreme can lead to 'patchy' lithography, particularly for shorter gate length devices. This effect is readily observed by performing a gate recess etch which highlights the areas of underexposure after resist removal (Fig 1).

METHOD

Such variations in gate lithography can be reduced by adopting a process in which the gate level is defined prior to the ohmic contacts, allowing the gate resist to be spun across a planar surface. However difficulties then arise in the ability to produce low resistance ohmic contacts (which require thermal annealing) without adverse degradation to the Schottky behavior of the gate contact [2].

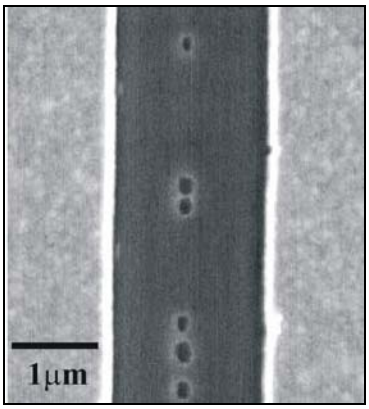

Fig 1. Patchy gate recess etch between source - drain metallisation

As described in this work, this problem is overcome with the development of a non-annealed ohmic process with which low resistance ohmic contacts are realised without subjection of the gate to high annealing temperatures [2]. The ability to form these low resistance contacts relies on the tailoring of the material band structure through the introduction of an additional layer of delta doping [3]. Vertical conduction through the material layers between the ohmic metallisation and device channel is then maximised without the need of annealing.

The basic InP HEMT material structure used for this process is given in Fig 2. Proper situation of the additional layer of delta doping within the barrier layer of the material minimises the magnitude of the potential barriers that arise vertically though the structure. Thus the impedance vertically through the material structure is reduced. This is carefully balanced to avoid parasitic conduction through the material layers adjacent to the channel which acts to degrade device performance.

Using the non-annealed ohmic process a figure for the vertical contact resistance of 0.15Ω.mm is extracted from recessed TLM measurements [4]. Beyond this low contact

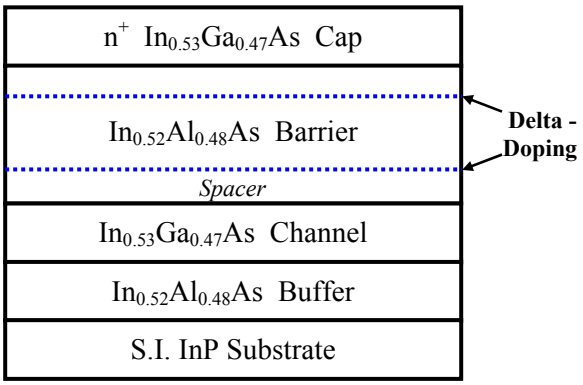

Fig 2. Double delta doped InP HEMT material structure

resistance figure, the addition of the second layer of delta doping also acts to reduce the magnitude of the parasitic access resistances into the intrinsic device region. Reduction of these parasitic resistances is found to increase device performance particular for properly scaled shorter gate length systems [5].

DEVICE FABRICATION

Devices with 70nm T-gates were fabricated using the material structure given in Fig. 2 and using the non-annealed ohmic process as follows:

To electrically isolate and define the active geometry of the device an orthophosphoric based wet mesa etch was initially performed. Reversing the ohmic and gate levels from the standard process flow, the 70nm T-gate level was performed next. This relied upon the definition of the T-gate profile into a PMMA/LOR/UVIII resist stack at 100keV using a Leica EBPG5-HR 100 electron beam lithography tool. A succinic acid based double gate recess etch then allowed metallisation of the Ti:Pd:Au gate onto the InAlAs barrier layer (Fig 3). Deposition of a Ni:Ge:Au based ohmic metallisation at a separation of 1.6um to either side of the gate then formed the device source and drain contacts. Finally coplanar waveguide bondpads were defined to allow on-wafer DC and RF characterization.

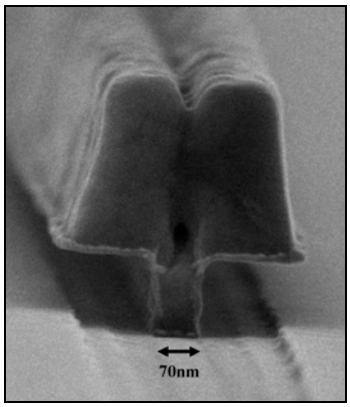

Fig 3. Metallised 70nm T-gate with double recess etch

DEVICE CHARACTERISATION

Following the fabrication of varied width 70nm devices, each was characterised at DC to examine the yield and consistency of operation across the range of devices. This indicated excellent device yield for each device width (Fig 4) with little evidence of variable gate lithography as indicated by the threshold voltage distribution across all operational devices (Fig 5).

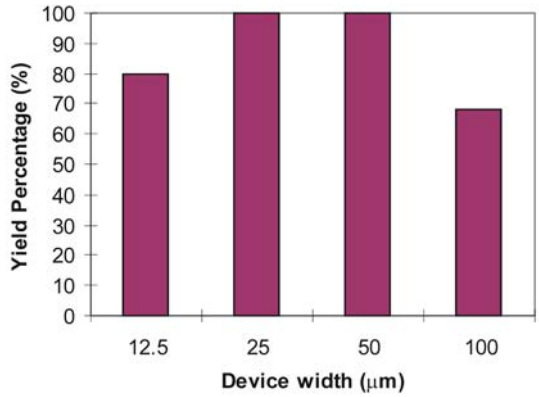

Fig 4. Measured device yield vs. device width

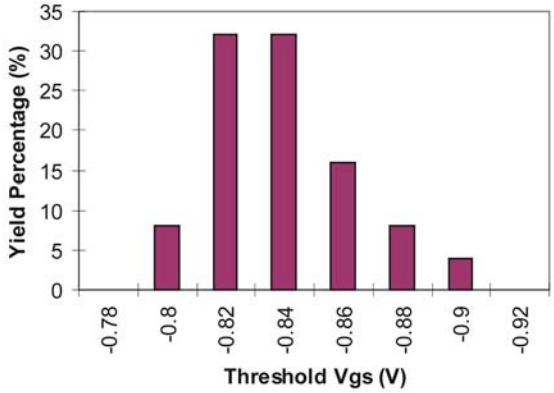

Fig 5. Threshold voltage distribution

Upon inspection of the non-operational devices it became evident that in most cases damage to the gate in some form was responsible. This was also found to occur predominantly with the devices situated towards the edge of the wafer and hence could arguably be due to handling of the wafer through the fabrication process. Closer inspection of a non-operational device in which the gate has separated from the device surface leaving the recess etch visible demonstrates the linearity of the etch along the width of the device (Fig 6). Again this can be compared with the extreme case given in Fig 1, contrasting the difference between defining the gate onto a planar surface and within a source-drain gap.

The consistency of performance across the operational devices also reflects the lack of deviation in the gate profile

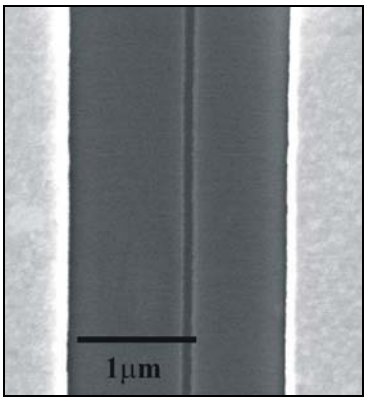

Fig 6. Clear gate recess etch between source - drain metallisation

as indicated by the threshold voltage distribution. As demonstrated in Fig 5, the majority of devices exhibit a threshold voltage within the –0.82V to –0.86V range, demonstrating a standard deviation of 0.024V.

Beyond the statistical variation observed, the devices exhibited excellent DC characteristics including peak extrinsic transconductance figures in the range 1350mS/mm and a drain saturation current in the range 800mA/mm. Standard device output and transfer/transconductance characteristics are given in Figs 7 & 8 respectively. This performance can be attributed to the increased carrier concentration from the second layer of delta doping in addition to a reduction in the device access resistances through parallel conduction [3].

Device S-parameters were taken across a range of bias points to allow the extraction of accurate figures of merit for the RF performance of the devices. These produced peak figures of 255GHz for the cut-off frequency f_T, and 240GHz for the maximum frequency f_{max}.

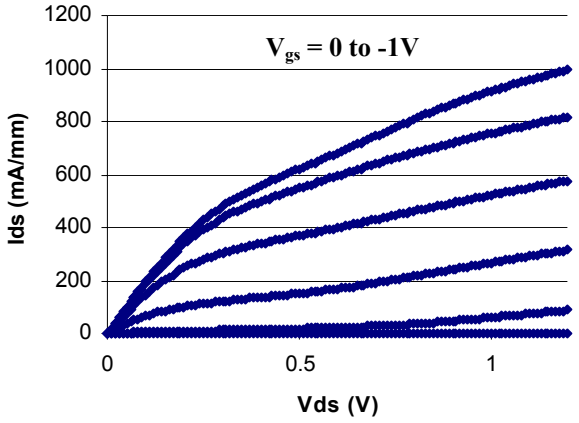

Fig 7. 70nm I_{ds} - V_{ds} device characteristics with threshold voltage ~ - 0.85V V_{gs}

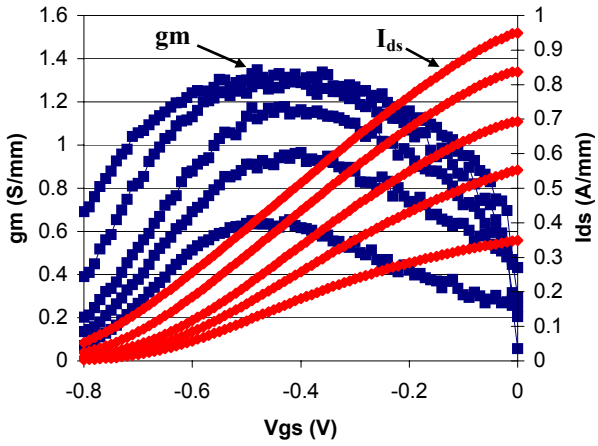

Fig 8. 70nm transfer (Ids) and transconductance (gm) characteristics for stepped source-drain bias 0.2 to 1V Vds.

CONCLUSIONS

By developing a non-annealed ohmic contact process for use in a 70nm InP HEMT process flow, the variation often observed in the gate lithography along the width of the device is avoided. This stems from the ability to define the gate level upon a planar surface and hence eliminates resist fluctuations that arise from being spun between the source and drain contacts. For shorter gate lengths (sub100nm) this process becomes crucial for consistent device operation as fluctuation in gate geometry will impact such ultra-short gate length systems more severely.

In addition to providing a route to improving consistency in device operation for short gate length systems, the use of the non-annealed process also benefits the device performance. As has been reported previously [3], reduction of the parasitic access resistances as a side effect of the non-annealed process acts to improve device performance, particularly for shorter gate lengths. This also provides a route to the realisation of a self-aligned gate process in which these parasitics are further reduced, further improving device performance.

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ACRONYMS

HEMT : High Electron Mobility Transistor
PMMA Poly-Methyl Methacrylate
LOR : Lift-off resist
UVIII : Ultra Violet III
DC : Direct Current
RF : Radio Frequency