Interlayer and Intershot Charging-Induced Pattern Distortion on GaAs Substrates Exposed with a High Throughput Shaped Beam Electron Beam Lithography System

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Keywords: Electron beam lithography, charging, t-gate, overlay, pattern distortion, Espacer

Abstract

Electron beam lithography is a viable option for exposure of high-resolution patterns such as t-gates in GaAs manufacturing, in part due to the speed and ease of use of modern electron beam direct write tools. In order to achieve greater speed, these tools utilize higher beam current densities and variable shaped beams. The resulting higher beam currents at the resist surface, however, can create significant amounts of pattern misplacement due to resist charging effects. In many cases, the misalignment results in unacceptable layer-to-layer overlay and a lower yielding process. Understanding the amount of charging, its effects on a process, and how to minimize the effect are keys to maintaining a high-throughput t-gate process. This paper will present quantitative results of charging effects on semi-insulating, ion implanted, and pHEMT GaAs substrates. We show that a polymeric anti-charging layer is effective in reducing pattern displacements to an acceptable level, even in the extreme case of the exposure of semi-insulating substrates.

INTRODUCTION

Vast improvements have been made to increase the throughput of direct-write electron beam lithography (EBL) systems, including many such improvements that are included in the Hitachi HL-800 series of tools [1]. These improvements include traveling wafer stages, variable shaped high current density beam guns, fast multi-tiered deflection systems, and fast beam blankers. In order to take advantage of these improvements, considerations must be taken to minimize or eliminate charge-induced pattern distortion and displacement. This paper will quantitatively present the effects of shot-to-shot and layer-to-layer charging effects on GaAs direct write patterns, as well as techniques for minimizing those effects in our process while maintaining high throughput.

EXPERIMENTAL SETUP

The exposure tool utilized for the e-beam exposures was a 50 keV Hitachi HL-800D used in traveling stage mode. The system is a variable shaped beam tool with a maximum shot size of 4 um. We exposed patterns on semi-insulating (SI), ion implanted, and pHEMT GaAs wafers using PMMA that in turn was developed using a mixture of isopropyl alcohol (IPA) and methyl isobutyl ketone (MIBK). Table 1 summarizes the process conditions and sheet resistivity values for each substrate and pattern.

TABLE 1
Process Condition Summary

Pattern	GaAs Substrate	Sheet Resistivity (Ω/□)	Resist Thickness (Å)	Dose (μC/cm^2)
Box-in-bar	Semi-Insulating	~10^{10}	2200	~300 & ~2300
Box-in-bar	Ion Implanted	300	2200	~300 & ~2300
Overlay	pHEMT	150	various	~300

Box-in-Bar Pattern

A box-in-bar pattern with 3 separate layers was used to measure gross pattern displacement (Figure 1). Pattern 1 (1) of the box-in-bar pattern is a square ring with inner dimensions of 40x40um, pattern 2 (2) is a 100x100um square, and pattern 3 (3) is a 20x20um square centered within 1. To examine charging effects in exposures the reference box, 1, was exposed first followed immediately by pattern 2. The interior box, 3, was exposed last following a 15 second delay. The pattern layout was a 5x5 array in a 6000x6000um reticle.

The HL-800D has a three-tiered deflection system consisting of a main (maximum 5000um) deflection system, a medium or sub-field (maximum ~500um) deflection system, and a dynamically varying fine or sub-sub-field (maximum ~50 micron) deflection system. Care was taken in all the pattern designs described here to prevent or at least minimize the impact of stitching and field boundaries on the charging results, including location of the critical pattern 3 described above within a single sub-sub-field.

The patterns were exposed, developed, and then visually inspected and measured. An OSI Metra 2000 provided automated metrology measurements across the 100mm wafers and was used to characterize charging-induced pattern displacements down to approximately 0.10 microns. Higher resolution measurements, necessary in the case of pHEMT wafers that were exposed using anti-charging layers, necessitated the use of the EBL tool itself to characterize the charging effects. This was done by returning the wafers, after metal liftoff and resist strip, to the tool where its automated marker location capability could be utilized to measure displacements down to the ~10nm range. These

measurements required the use of specially designed markers that will be described in a later section.

Distance From Grounding Pin

Some simple experiments showed the effects of gross charging effects as well as the importance of macroscopic tool geometry on these effects, specifically, the effect of a single grounding pin that is located near the wafer flat on the HL-800D 100mm wafer holder. For these experiments, semi-insulating and implanted wafers were exposed with the box-in-bar pattern in exposures that progressed from left to right on the wafer beginning at the bottom of each reticle column. This is the typical mode of exposure of the tool. Figure 1 shows the pattern distortion of two chips from the same semi-insulating wafer that varied only in their distance from the grounding pin. The chip furthermost from the grounding pin exhibits severe pattern distortion, even within each layer (Figure 1a). Not only are the respective patterns 1, 2, and 3 misplaced with respect to each other due to charging effects but the structures themselves show significant intershot distortion due to the misalignment of single shots of the variable shaped beam (VSB) system. Interestingly, the chip closest to the grounding pin had very little visible intershot pattern distortion (Figure 1b). The intershot pattern distortion is minimal for this chip but has not been completely eliminated.

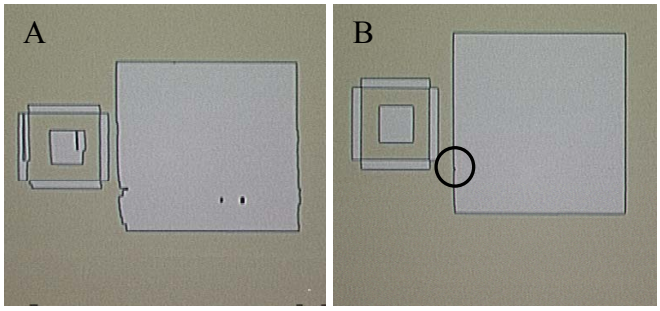

Figure 1-Comparison of two chips from the same semi-insulating wafer.
A) Chip located furthest from the grounding pin. Each pattern layer exhibits dramatic distortion. In addition, pattern 3 is shifted away from center.
B) Chip located close to grounding pin. Intershot pattern distortion is minimized, but not eliminated (circled area has a slight defect). Pattern 3 is visibly centered.

The exposure of semi-insulating wafers without any anti-charging layer is obviously an extreme case of EBL charging. However, it is instructive to note that the location of the grounding pin was also noticeable in the distortion maps of higher conductivity wafers (pHEMT, for example) with distortions that were an order of magnitude lower than the effects described for SI wafers.

Espacer

One way of controlling charging effects is by adding an anti-charging layer on top of the resist system. This is often accomplished by the deposition of a thin (<0.10um) layer of metal that is subsequently stripped before development of the resist. In this work, however, we used a layer of commercially available polymeric thin film (Espacer) to reduce charging. Espacer is a water-soluble conducting polymer with ~MΩ/□ sheet resistivity that was designed for charge dissipation in ebeam lithography [1,2]. Measurements of wafers exposed with and without Espacer were a good test of the effects of electron-beam induced charging; the pronounced effect of the Espacer layer in all cases was consistent with the placement errors being due to charging rather than local heating effects by the beam.

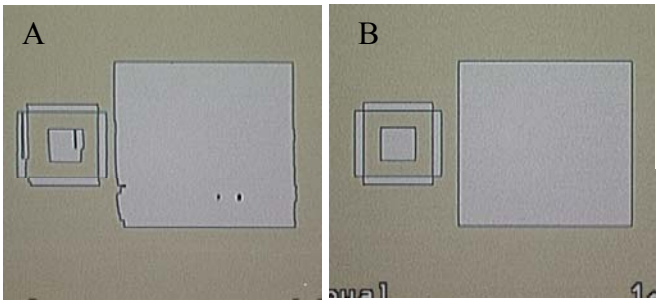

Figure 2-Comparison of the pattern distortion between two semi-insulating wafers, one each with and without an Espacer coating. The chips shown are the same chip position, *i.e.* row/column number is the same. A) Chip from a wafer exposed without an Espacer coating. The pattern has been greatly distorted, even within a single layer. B) Equivalent chip on a wafer coated with Espacer before exposure. The pattern is sharp with no visible distortion.

Figure 2 shows the difference in pattern distortion between two semi-insulating wafers exposed with our box-in-bar pattern, with and without Espacer. The same chip position is pictured on each wafer. The wafer coated with Espacer exhibits no discernible distortion, even on chips located far from the grounding pin. On semi-insulating substrates without Espacer the measured pattern displacement was significant (~0.20um) and tended to become more variable with the distance of the die from the grounding pin (Figure 3). With an Espacer coating, even semi-insulating substrates at large exposure doses exhibited acceptable pattern displacement of 0.10um or below. As can be seen from Figure 3, EBL-induced charging often manifests itself as a

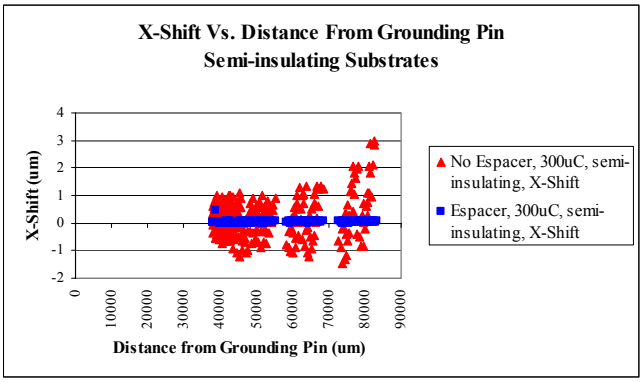

Figure 3-X-pattern displacement, as measured on the OSI Metra tool for semi-insulating substrates with and without Espacer coating during exposure. The wafer without Espacer, red triangles, exhibits a great variation in pattern displacement, both positive and negative. The wafer with an Espacer coating did not exhibit this behavior, even on a finer scale.

variation (or scatter) in pattern misplacement rather than any systematic shifts that depend completely on local geometry (i.e., the test structure described above).

Ion-implanted substrates had moderately acceptable pattern displacements of ~0.15um or less as measured by the OSI Metra tool regardless of dose or Espacer coating. The smaller effects in this case, and in the case of pHEMT wafers, made it necessary to develop a technique capable of higher resolution.

Overlay marker search pattern

The effects of charging-induced pattern distortion in the EBL exposure of ion implanted or pHEMT epitaxial wafers proved difficult to characterize using the optical Metra tool due to the relatively small resulting displacements (<100nm). Consequently, we used the ability of the HL-800D to measure partial alignment markers arranged in a pattern to test the overlay capability of the tool. The overlay pattern designed by Hitachi is a series of partial alignment markers printed in 2 layers; we exposed the first layer using an optical I-line step-and-repeat exposure system and the second with the HL-800D. The second layer is the other half of the alignment marker, which in the absence of charging effects would line up with the first layer creating a continuous alignment mark. Upon exposure and development of layer 2, the pattern was metallized, lifted off, and the resist removed. The HL-800D tool measures the pattern displacement as shifts of the layer 2 marker positions from the intended position, and it conveniently produces a graph of vector displacement as a function of measurement position across the wafer. We did not attempt to subtract any errors due to general stepper-to-e-beam matching from the data since they were of generally lower level (<50nm) and tended to be averaged out of the wafer data.

pHEMT wafers exposed without an Espacer anti-charging layer generally exhibited lower amounts of charging than their SI or implanted counterparts as would be expected based on their lower sheet resistance, but still exhibited similar effects. Table 2 summarizes the results in terms of wafer averages. With no anti-charging layer and the default exposure strategy, the placement error was unacceptable (~200nm mean plus three sigma) in both X and Y. Moreover, there was some dependence on the location of the grounding pin with respect to the overlay pattern metal in the underlying layers that led to large variances in the displacements. As a result, the numbers listed without Espacer in Table 2 should be considered typical results. Specifically, when the sample holder's grounding pin pushed through the resist and contacted an underlying metal finger the best results (lower distortions) were found. However, if the grounding pin did not touch underlying metal the results were highly variable (up to ~600nm distortions). This was somewhat similar to the case of SI wafers in the earlier section, in which charging effects (in this case, with no metal layers involved) were often highly variable and the distortion data contained considerable scatter. It also points to a source of variability due to the density of any underlying metal pattern.

TABLE 2
Summary of pHEMT overlay marker search pattern displacement measurements.

Anti-charging Layer	Exposure Strategy	X-Displacement mean + 3 sigma (nm)	Y-Displacement mean + 3 sigma (nm)
None	Default	250	146
None	Right to left, with a delay between reticle columns	100	101
None[1]	Left to right, with a delay between reticle columns	68	49
Espacer	Default	54	79
Espacer	Right to left, with a delay between reticle columns	77	84

[1]Result listed in table is from a wafer that had the grounding pin pushed through the resist and contacting layer 1 metal. Results without grounding pin contacting metal were varied with the worst X-pattern displacement = 600nm and the worst Y-displacement observed = 140nm.

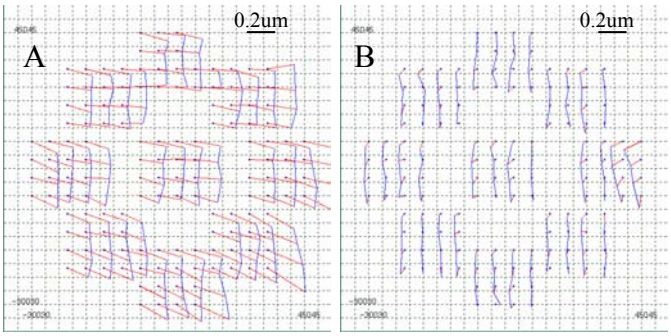

Figure 4-Comparison of pattern placement errors on pHEMT wafers for wafers both using the default exposure strategy. The red lines are vectors showing the displacement of the pattern from the designed location. A) Wafer exposed with no anti-charging layer. B) Wafer exposed using Espacer as the anticharging layer.

As expected the addition of Espacer improved the distortion results dramatically. Figure 4 shows a comparison of the tool-generated distortion maps between no Espacer (left) and Espacer (right). Not only did the measured distortions drop by nearly a factor of 3x using the anti-charging layer, but the reproducibility of the results also improved greatly. We suspect that while the direct drainage of EBL-induced charge is a major effect of Espacer, an associated (and important) effect of the use of the layer is

also a higher repeatability of the ground pin to wafer electrical contact.

To shed further light on effects with no applied anti-charging layer we varied the manner in which the wafer was exposed. The HL-800D's default exposure strategy is from left to right on the wafer, generally towards the grounding pin, starting at the bottom of each column of reticles and moving the stage in the y-dimension during actual exposure of the pattern. Changing the exposure strategy both in direction and speed reduced the placement error dramatically (Table 2), sometimes approaching the low level of distortion achieved with Espacer. Interestingly, exposing the wafer in a right-to-left fashion, generally away from the grounding pin, also led to much better results. We believe that this is due to a combination of two effects. First, exposing the wafer in this manner slowed the exposure somewhat, allowing residual charge to drain. This would lead us to conclude that the decay time of the residual charge has a time constant on the order of a few minutes. Also, beginning the wafer exposure near the grounding pin could help drain induced charge early in the exposure and helped avoid the rise of local voltages (~10s of volts) near the area under exposure by the beam.

Another experiment that intentionally slowed the exposure (see Table 2) resulted in significantly lower displacements as compared to other results from omitting Espacer, confirming that the time constant of the decay of the induced charge is critical to the effects we observed. Utilizing Espacer, writing a wafer from right to left including a delay was comparable to the default exposure mode as expected, consistent with a highly effective drainage of induced charge and a reproducible contact of the wafer surface to the grounding pin.

CONCLUSIONS

Modern electron beam direct write tools offer the potential for high-speed GaAs manufacturing throughput as a result of high beam current densities, high frequency deflection systems, and fast sample stages. However, pattern displacements due to charging issues in these tools can be significant (>200nm) and is a strong function of substrate type, writing speed and system geometry effects such as the location of wafer grounding pins. The decay time of these charging effects appears to be on the order of minutes and can interact with writing direction and strategy. We demonstrate that the addition of a polymeric anti-charging layer of sheet resistance ~1 MΩ/□ to a typical resist system is highly effective in reducing these charging effects to the sub-100nm level and is key to obtaining high pattern quality with no associated increases in EBL write times.

ACKNOWLEDGEMENTS

The authors would like to thank Dr. Hiroyuki Ito and Genya Matsuoka of Hitachi for sharing their insight regarding wafer-grounding issues of the HL-800D. Thanks as well to Jim Halvorson, Vicki Milam, Susan Paine, and Robert Turner at TriQuint Texas who contributed greatly to this work with the fabrication of countless test wafers.

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ACRONYMS

pHEMT: pseudomorphic high electron mobility transistor
EBL: electron beam lithography
IPA: isopropyl alcohol
MIBK: methyl isobutyl ketone
PMMA: polymethyl methacrylate
VSB: variable shaped beam