Cost Effective T-Gate Process for PHEMT-based MMIC with Large Gate Periphery

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Abstract

One of the major yield killers of power-amplifier PHEMT-based MMICs is fabricating a T-shaped gate with gate periphery of several tens of mm. We have investigated a novel PMMA/PMGI/PMMA tri-layer resist scheme for T-Gate definition of PHEMTs with 0.25-µm gate length and in-situ Ar^+ ion beam treatment before gate evaporation as methods for eliminating this problem. We intend to extend this technology for devices with shorter gate length (L_g).

INTRODUCTION

Fabrication power-amplifier PHEMT-based Monolithic Microwave Integrated Circuits (MMICs) with high yield is a challenging task. Conventional tri- or double-layer approaches for T-gate implementation on typically rely on resists with different sensitivities and exposure strategy based on writing, "foot" and "wing" patterns. [1] We suggest a new method of fabricating T-Gates by exposure of single line (foot) by electron beam lithography using a tri-layer resist structure with a PMGI layer in between two layers of PMMA. For strong adhesion between the gate and the GaAs we use an Ar^+ ion treatment to activate the GaAs layer.
Application of any kind of plasma treatment in the vicinity of a PHEMT channel can raise concerns about plasma damage. We present a study of impact of Ar^+ ion energy on the Schottky diode electro-physical characteristics and transistor performance.

TRI-LAYER RESIST PROCESS FLOW

1) Figure 1 summarizes the tri-layer resist process flow for the T-Gate fabrication. The combination of e-beam sensitive resist consists of 220 nm thick bottom layer of PMMA, an 800 nm thick middle Polydimethylglutarimide (PMGI) layer with another 170 nm thick PMMA layer on top. PMGI is an electron and photon sensitive resist with unique properties that makes it suitable for many lithographic applications. PMGI is virtually insoluble in typical e-beam resist solvents and thus can be used in a resist stack with no or negligible intermixing problems. PMGI is mostly soluble in standard alkaline photo-resist developers and has highly controllable dissolution properties, together with high thermal stability and superior planarization characteristics.

These attributes make PMGI uniquely suited for many critical lift-off applications. The gate was exposed in a single pass, which has a great potential for shorter gates since it eliminates parasitic influence of the "wing" exposure on the "foot" opening. In our previous work, we found that the "wing" adds to the "foot" between 25%-50% of L_g, depending on "foot" size.
An additional advantage of this method is a reduction of writing time by 40% per wafer.

2) The final T-Gate lift-off structure is formed by a series of independent selective development steps. The top two layers form a reliable overhanging structure for metal liftoff. The top PMMA layer line width determines the cross-sectional width of the top cap. This layer develops by pure MIBK. The line width of the top PMMA stays untouched by the developing process of the PMGI by 400K developers. The contrast curves for both PMMA and PMGI illustrate excellent selectivity of the respective developers [1]. The bottom layer of the PMMA develops in a sensitive

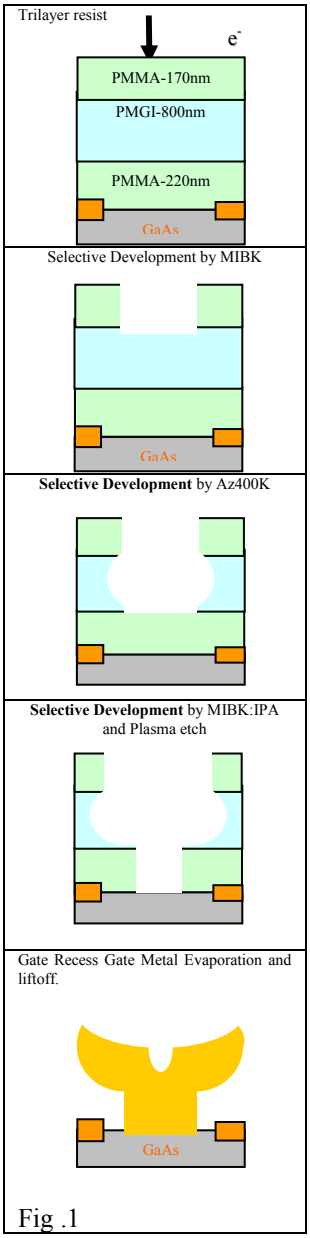

Fig .1

developer mixture of MIBK:IPA 1:3, which provides high resolution of CD (Lg). During the development of the bottom PMMA layer no further development of the top layer is expected (since this layer be overdeveloped at the first step). Thus, the top dimensions are retained. We note that unexposed PMGI exhibits a rather high dissolution rate in tetra-methyl ammonium hydroxide solution (up to 140 nm/min). Thus, the actual exposure dose of PMGI is not critical. The degree of undercut can be controlled by the development or dissolution time of the PMGI layer with no additional development of the other layers.

3) After the developing process, the resist stack is exposed to oxygen plasma for a short cleaning process followed by gate recess formation.

4) The final step is gate evaporation.
Fig. 2 shows the tri-layer resist T-Gate.

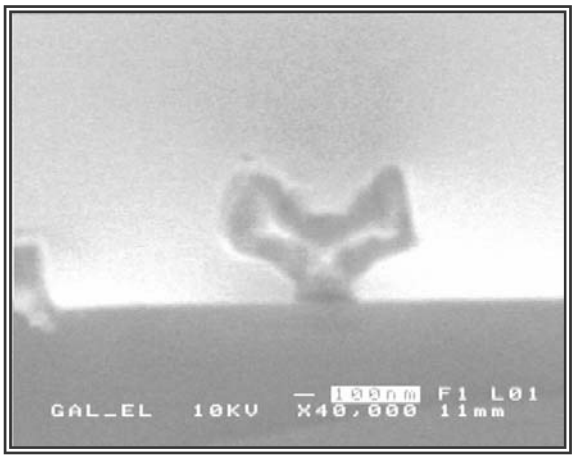

Fig.2. A tri-layer 0.25 μm T-Gate.

ION BEAM TREATMENT

1) The Ar^+ ion beam gun is located in the evaporation chamber. After wet etching, there is always a possibility of some water vapor or other residual monolayers at the surface of the opening channel. This affects the adhesion of the evaporated gate metal to the GaAs. Elimination of the adsorbed layers improves the adhesion, resulting in better yields. This treatment shows a significant improvement in gate yield (up to 95%). At certain ion energies (see next subsection) there is no significant impact on the device electrical performance.

2) Samples of bulk resistor structures with recessed channels have been exposed to Ar^+ ion flux at various ion energies. We measured the Idss current reduction after this treatment. The saturation drain-source current – Idss has been measured as a function of the Ar^+ ion energy. Below 100 eV of ion energy there is no reduction of Idss. We have continued our study with samples treated at these energies.

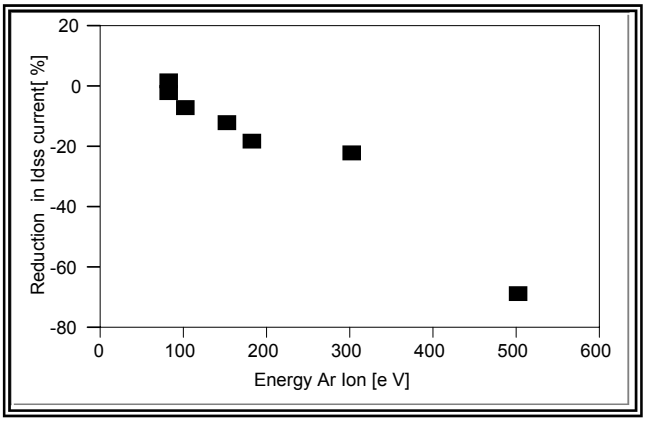

Fig. 3. Idss as a function of Ar^+ ion energy

3) We examined the Ar^+ ion flux treatment effect on the Schottky diode (Table 1) and transistors (Table 2). Wafers 088 and 090 underwent a baseline process while wafers 092 and 100 Ar^+ ion treated at energy sufficient for surface activation.

4) We have checked the Schottky diode leakage current Ig at Vgs= –9 V. Table 1 presents the changes in median Ig of devices that underwent Ar+ treatment compared to the baseline process. We define yield as percentage of transistors that may be completely closed down to 1mA/mm. There seems to be no major difference in diode leakage currents but the yield has been significantly improved.

Wafer	Mean	Std Dev	Yield
088	-0.169	0.06	60%
090	-0.176	0.07	72%
092(Ar)	-0.111	0.06	98%
100(Ar)	-0.104	0.10	98%

Table 1. Gate leakage current Ig (mA/mm) at Vgs=- 9 V for devices with and without Ar^+ treatment.

5) The transistor off-state breakdown voltage Vb(off) was measured, when the drain voltage was swept from Vd=0 to 18 V and the gate voltage was Vgs=-2V so the transistor was off. The drain and gate current was monitored and breakdown voltage was reached when the current was raised up to 1mA/mm. Table 2 shows a slight improvement in the mean Vb(off) of transistors that underwent Ar^+ treatment as compared to base line process.

Wafer	Mean	Std Dev
088	16.3	0.4
090	16.6	0.8
092	17.6	0.1
100	17.7	0.2

Table 2. Transistor off-state breakdown voltage (V) for devices with and without Ar^+ treatment.

6) Gm profile curves (see Fig. 4) did not show any effect of Ar^+ treatment.

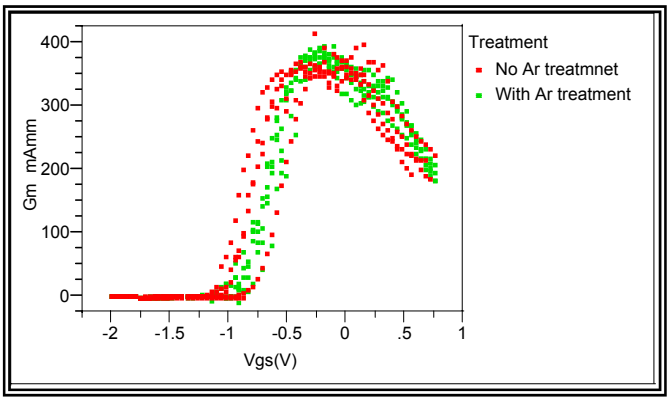

Fig. 4. Gm as a function of Vgs for devices with (green dots) and without Ar^+ treatment (red dots).

7) we have looked for changes in the maximum available gain (MAG) at 10 GHz and F_T of the transistors. and there was no observable impact of Ar+ treatment too (Fig.5,6).

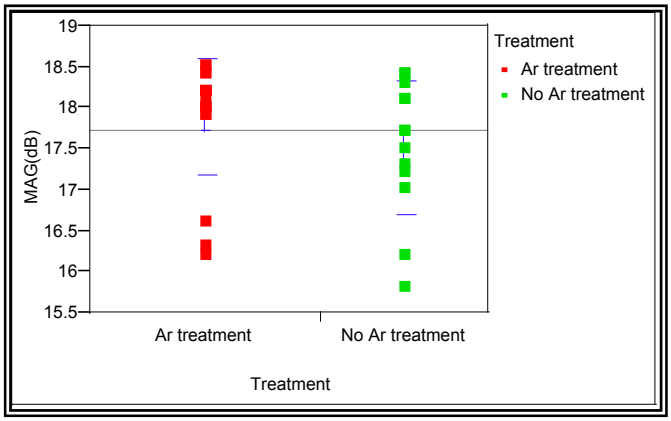

Fig.5 The MAG changes on transistors that pass Ar+ treatment (Red) and transistors without Ar+ treatment (green).

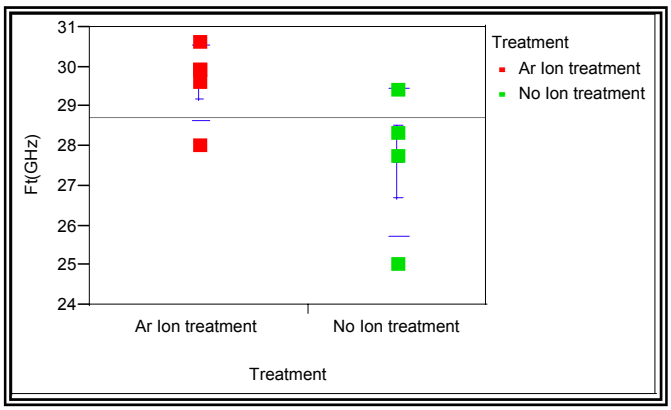

Fig .6 The F_T changes on transistors that pass Ar+ treatment (Red) and transistors without Ar+ treatment (green).

Means and Std Deviations for Ft:

Treatment	Mean (GHz)	Std Dev
Ar+ Ion treatment	29.6000	0.96695
No Ion treatment	27.6000	1.87083

Table 3 Ft Mean and Std.Dev of transistors with and without Ar+ Ion treatment.

Conclusions:

Fabrication of power amplifier MMICs based on PHEMTs with novel PMMA/PGMI/PMMA tri-layer resist and in-situ Ar+ ion treatment before gate evaporation improve the total device yield. This technology provides manufacturing cost reduction because shorter e-beam writing time and implementation of only two types of resists: PMMA and PMGI. We intend to extend this technology for devices with shorter gates.

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ACRONYMS

FET: field effect transistors.
MMIC: Monolithic Microwave Integrated Circuited.
MAG: Maximum Available Gain