Manufacturable AlSb/InAs HEMT Technology for Ultra-Low Power Millimeter-Wave Integrated Circuits

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Abstract

High electron mobility transistors with InAs channels and sub 0.1-μm metal gates, have demonstrated a 100% improvement in low-power, high-speed figure of merits over conventional InAlAs/InGaAs lattice-matched HEMTs and MHEMTs. AlSb/InAs MHEMTs exhibit transconductances as high as 1.3 S/mm at drain biases as low as 0.3 V, while maintaining f_T and f_{max} results greater than 220 GHz and 270 GHz, respectively. In this paper, we will discuss our efforts to develop this technology for revolutionary low-power, high frequency MMIC applications.

INTRODUCTION

Monolithic Millimeter-wave Integrated Circuits (MMIC) based upon InAs-channel HEMT's have the potential to enable revolutionary low-noise, low-power, and high-speed applications. As shown in Table 1, InAs electronic properties, such as electron mobility and peak velocity, are nearly two times larger as compared to state-of-the-art $In_XGa_{1-X}As$-channels.

InAlAs/InGaAs HEMT's grown on lattice-matched InP substrate offer the best combination of low-power and low-noise MMIC's to date [1-2]. Based on our device data, as shown in Figure 1, we estimate InAs-based HEMT performance meets or exceeds InAlAs/InGaAs HEMT but with only one-tenth the power dissipation.

However, development of InAs channel devices is challenging because of the lack of viable semi-insulating substrates for lattice-matched growth. Metamorphic growth using the $Al_XGa_{1-X}Sb_YAs_{1-Y}$/InAs material system, which has a lattice constant near 6.1 Å, as shown in Figure 2, has proven to be a viable alternative for state-of-the-art InAs-channel HEMTs [3-5] and researchers in this field now routinely achieve electron mobility > 15,000 cm^2/V-s with tensile strained InAs channels. However, the approach does hold several unique challenges such as intrinsic material stability, gate leakage, and yield limiting defect densities, which have been incrementally addressed over the years [6]. Only recently have the first AlSb/InAs MHEMT based MMIC's been demonstrated [7,8].

In this paper, we will discuss the successful development of a manufacturable AlSb/InAs MHEMT technology at Northrop Grumman Space Technology (NGST) and Naval Research Laboratory (NRL) for ultra low-power, high frequency MMIC products.

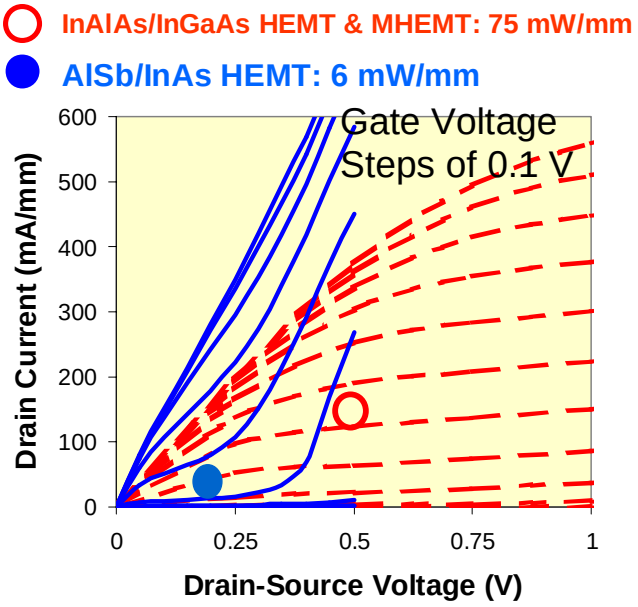

Fig. 1 AlSb/InAs HEMT (solid) bias points for minimum noise figure and lowest DC power dissipation, compared to InAlAs/InGaAs HEMT (dashed). Curves displayed for gate voltage step of 0.1 V.

Table 1. HEMT Channel Electron Transport Properties

Property	InAs	$In_{0.53}Ga_{0.47}As$	GaAs
m_e*	0.023	0.041	0.067
μ (cm^2/V-sec)	20000	8000	4500
Peak velocity (10^7 cm/sec)	4.0	2.7	2.2
Γ-L valley seperation (eV)	0.9	0.55	0.31
Band Gap (eV)	0.36	0.72	1.42

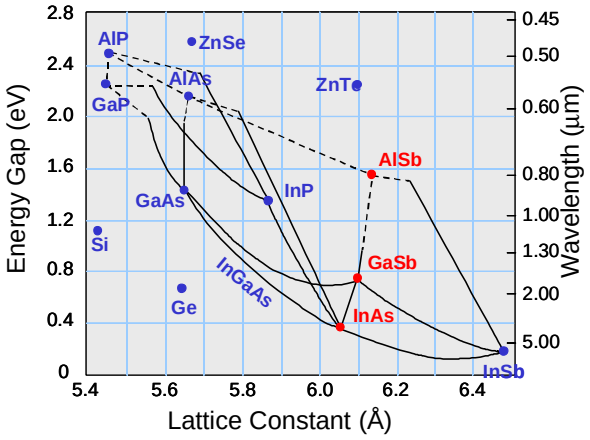

Fig. 2 The $Al_XGa_{1-X}Sb_YAs_{1-Y}$/InAs material system and approximate 6.1 Å lattice constant

DEVICE GROWTH & FABRICATION

The AlSb/InAs structures were grown by molecular beam epitaxy (MBE) on semi-insulating 3" GaAs substrates, and both NGST and NRL labs have grown several wafers of a standard structure, as shown in Figure 3, to qualify the transference of growth and frontside process methodology, as well as comparative analysis.

Layer	Device	Thick. (Å)	Doping
	LOW-NOISE		
Cap	InAs	20	
Hole Barrier	$In_{0.40}Al_{0.60}As$	40	
Electron Barrier	AlSb	12	
Doping	InAs-Si	12	3e19 (Si)
Electron Barrier	AlSb	75	
Channel	InAs	150	
Back Barrier	AlSb	500	
Buffer Cap	$Al_{0.70}Ga_{0.30}Sb$	3000	
Relaxed M.M. Buffer	AlSb	17000	
GaAs Buffer	GaAs	2300	
Substrate	GaAs	----------	S. I.

Fig. 3 Layer structure of one standard profile grown at NGST and NRL

Both labs schedule destructive Hall measurements of as-grown standard profile wafers and perform non-destructive sheet resistance mapping on every grown wafer for statistical process control monitoring (SPCM). According to SPCM statistics, our standard profile grown obtains an average sheet resistance of 180.5 Ω/sq with less than 2.6% non-uniformity and 300K mobility of 19,100 $cm^2/V*s$ with electron sheet density of $1.77x10^{12}$ cm^{-2}. The fact that state-of-the-art growth of $Al_XGa_{1-X}Sb_YAs_{1-Y}$/InAs HEMT profiles can be successfully controlled in both research and pre-production MBE reactors is a testament to its reproducibility. Detailed technical rationale regarding the implementation of the hole barrier, doping plane, and buffer cap in our standard profile can be found in previous publications [3,4,9].

Furthermore, by optimizing MBE flux conditions and modulation doped methodology, the same profile obtains an average sheet resistance of 200.9 Ω/sq with less than 2.6% non-uniformity and 300K mobility of 26,300 $cm^2/V*s$ with electron sheet density of $1.28x10^{12}$ cm^{-2}, as shown in the trend chart of Figure 4. This combination of over 30% higher mobility and lower sheet charge provides better characteristics for ultra-low power circuit applications. The device pinch off voltage becomes more positive, while access resistance increases only marginally.

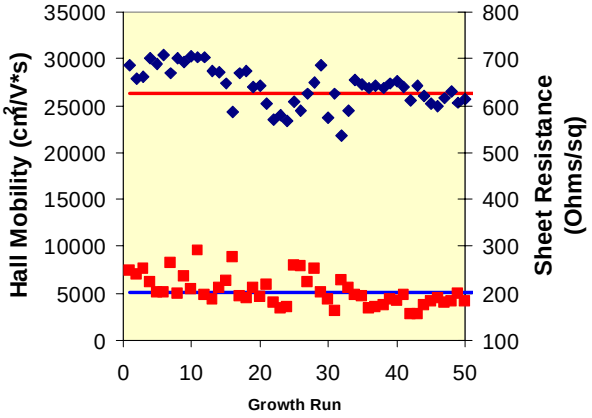

Fig. 4 Statistcal process control data for 50 epitaxially grown 3" wafers (Triangles) 300 K electron hall mobility (Squares) sheet resistance.

NGST's fabrication process uses qualified InP-HEMT production optical-stepper lithography, cleaning procedures, SPCM testing, and database tracking. Active device mesas were formed by using a BCl_3/Ar-based Inductively-coupled Plasma (ICP) etch to remove 1250 Å of the structure. The mesa isolation process was designed to end in the $Al_{0.7}Ga_{0.3}Sb$ layer, and achieves an average of 100 MΩ/sq of electrical isolation resistance without the need for implant isolation. This level of isolation is comparable to NGST's space-qualified, production InAlAs/InGaAs/InP HEMT's that employs both mesa isolation and implant isolation. Pd/Pt/Au ohmics alloyed at 175°C in a nitrogen atmosphere formed contacts with a resistance of 0.06 Ω-mm. Electron beam lithography was utilized to fabricate 0.1 µm Mo/Au T-gates in a 2 µm source-drain region. The source to gate distance was 0.8 µm.

Our MMIC integration process is identical to our flight-qualified InAlAs/InGaAs/InP HEMT process [10]. This process features devices and passive circuit components which are fully passivated with a total of 750 Å PECVD

SiN, two levels of interconnect metal including airbridges, 300 pF/mm^2 double-layer MIM capacitors with breakdown voltages over 100 volts, and 100-Ω/sq precision NiCr resistors with 0.6 mA/µm reliable operation.

Upon completion of frontside processing, wafers were thinned to a thickness of 100 µm. Round 40 µm diameter vias were etched through the substrate to allow contact from the HEMT source pads to the backside wafer ground plane.

RESULTS & DISCUSSION

Devices were DC tested on-wafer at the completion of processing. The devices displayed high transconductance (G_M) at low drain-source voltage (V_{DS}), and low on-state resistance (R_{ON}). The average G_M peak was 1.05 S/mm and 2.56 S/mm measured at a V_{DS} of 0.2 V and 0.4 V respectively. The average off-state reverse gate-drain breakdown (BV_{GDR}) was –1.42 V (measured at a gate current of -1 mA/mm). An example of the DC drain current (I_D) versus drain voltage (V_D) is shown in the top of Figure 5, while G_M vs. gate voltage (V_G) is shown in the bottom. DC characteristics in Figure 5 were measured from a 2-fingered 80-µm total gate periphery device, and illustrate the combined characteristics of low drain voltage operation, low knee voltage, and high transconductance, which are critical parameters for ultra-low power, high frequency operation. Device functional yields as high as 97% have been achieved for 3" wafers with excellent uniformity of DC characteristics, as depicted in Figure 6.

Small signal RF tests were also performed on-wafer, and maximum available gains greater than 10 dB at 100 GHz and f_{max} higher than 270 GHz were measured starting at V_{DS} of 0.4 volts and 112 mA/mm, as shown in Figure 7.

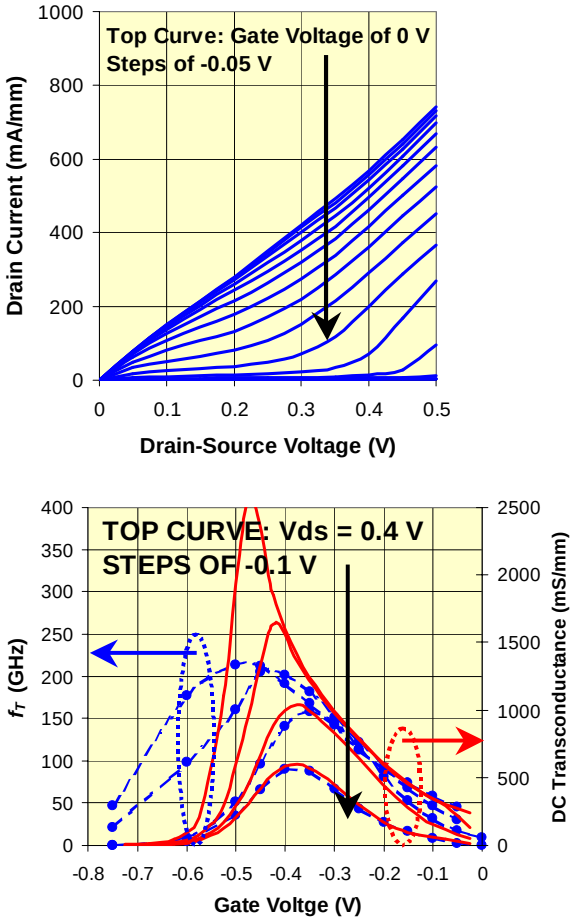

Fig. 5 Top: Measured drain current vs. drain voltage and Bottom: Extrapolated unity current gain frequency (dashed) and measured DC transconductance (solid) vs. gate voltage.

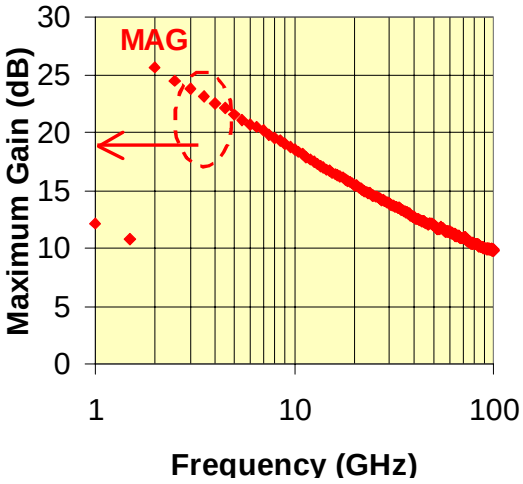

Fig. 7 Measured maximum available gain greater than 10 dB at 100 GHz for 2 x 40-µm devices.

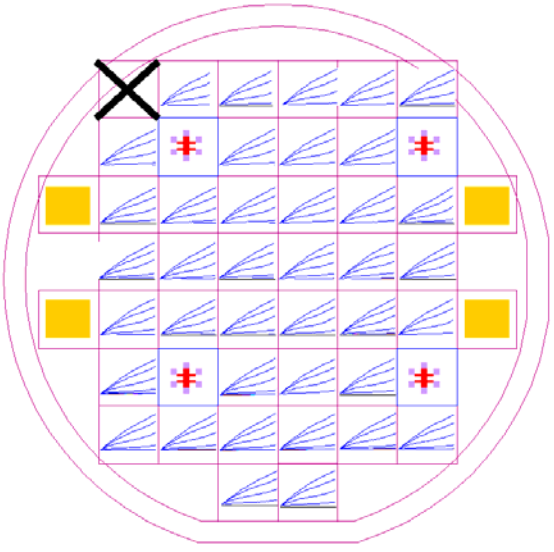

Fig. 6 Device yield of forty 4 x 75-µm devices across a 3" wafer depicted as location dependent DC-IV plots. Also drawn are four large-area hall bar, and four plating clip dropouts, and non-functional devices as "X".

The average peak f_T, was 153 GHz and 212 GHz at V_{DS} of 0.2 and 0.4 volts and drain current densities of 115 and 340 mA/mm, respectively. These correspond to DC power dissipations of 22 and 180 mW/mm. Compared to f_T-DC power performance of state-of-the art 0.1-µm gate length InAlAs/InGaAs/InP HEMT's, our AlSb/InAs HEMT's provide equivalent high-speed figure of merit performance at 5 to 10 times lower power dissipation, as shown in Figure 8.

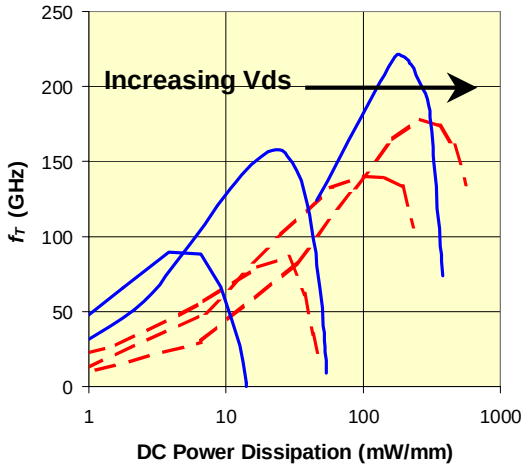

Fig. 8 Extrapolated unity current gain frequency vs. DC power dissipation for AlSb/InAs HEMT (solid) at VDS = 0.1, 0.2, and 0.5 volts and InAlAs/InGaAs HEMT (dashed) at VDS = 0.2, 0.5, and 1.0 volts.

Noise-pull tests were also performed on-wafer. As shown in Figure 9, at an ultra-low power dissipation bias of 6 mW/mm a minimum noise figure of 0.85 dB and associated gain of 11.5 dB was measured at V_{DS} of 0.2 volts. These minimum noise figures are comparable to state-of-art GaAs and InAlAs/InGaAs/InP HEMT's up to 26 GHz, but at 10 times lower power dissipation.

Conclusions

NGST and NRL have demonstrated a high performance and highly reproducible AlSb/InAs HEMT technology with revolutionary combined ultra-low power dissipation and excellent high-frequency performance.

Acknowledgements

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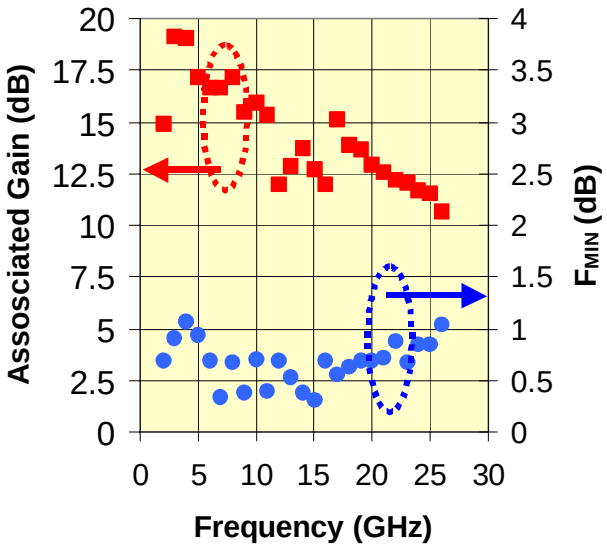

Fig. 9 Measured 2 to 26 GHz associated gain (G_A) and minimum noise figure (F_{MIN}) at V_{DS} = 0.2 volts and 6 mW/mm DC power dissipation.

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