Development of a GaN Transistor Process for Linear Power Applications

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Abstract

This paper provides an overview of the Nitronex power transistor process and discusses in detail the approaches taken to optimize performance for 28V linear applications. More specifically, key process performance metrics are traced through several generations of baseline process, highlighting some of the challenges met along the way, and concluding with a summary of product level performance achievements made possible with the current generation platform.

INTRODUCTION

The emerging third-generation (3G) wireless cellular networks are designed to provide high data rate services beyond traditional voice. To support these higher data rates, 3G air interfaces such as W-CDMA use variable amplitude envelope modulated signals with peak-to-average ratios of 8-12 dB, thus placing severe constraints on the linearity of the power amplifier and associated power transistors. On the base-station side, silicon LDMOS is the technology leader, owing to its excellent price-to-performance ratio compared to other commercially available technologies such as GaAs HFET and silicon BJT. While LDMOS has continued to evolve, AlGaN/GaN HFETs are beginning to show their long held promise as contenders for high-power transistor applications. With its superior material properties – critical electric field of ≥2 MV/cm and saturation velocity of $2.5x10^7$ cm/s – AlGaN/GaN HFETs significantly extend the design space of microwave power transistors. For example, typical AlGaN/GaN HFET structures achieve gate-to-drain breakdown voltages of approximately 70V/μm and current densities of 0.5-1 A/mm, resulting in power densities several times higher than commercially available devices. At the product level, these superior attributes translate into higher operating voltage, which simplifies system design, smaller chips, resulting in smaller packages, and higher devices impedances, enabling larger bandwidth matching circuits. Furthermore, early generations already show competitive device linearity, with further improvements foreseen for more advanced device structures.

Despite this promise, one factor that has limited acceptance of this technology has been the availability of high-quality substrate material of reasonable cost, quality, and size. Traditionally, GaN was grown on SiC or sapphire substrates. However, the high-cost, small substrate diameter, and in the case of sapphire, low thermal conductivity, make commercialization of high-power GaN devices on these substrates problematic. More recently, work has been undertaken to develop GaN device technology on large-area silicon substrates, which solves both the substrate diameter and cost issue associated with other substrates. We have also shown that the peak junction temperature follows a 1/x relationship with substrate thermal conductivity leading to diminishing improvements with better thermal conductivities [1], [2], [3]. Nitronex has developed a patented technology known as SIGANTIC™ that allows the growth of high quality GaN epilayers on silicon substrates [4]. Regarding cost, availability and process flexibility of this pervasive material, we feel this approach will prove to be enabling for commercializing gallium nitride device technology.

TECHNICAL APPROACH

A. The immediate economic advantage of silicon substrates

The economic advantage of silicon substrates has allowed Nitronex to produce a substantial volume of wafers during process development. During calendar year 2003, our fabrication facility processed over 1,100 AlGaN/GaN HFET wafers. A majority of these HFET wafers are processed through assembly. A selection of packaged devices from each wafer is subjected to extensive DC and RF testing. We have been able to clearly identify trends and establish correlations to performance and yield drivers that may have been lost to statistical variation in smaller sample sizes.

B. Benefits of a vertical organization

Nitronex has also benefited from the high degree of integration within our Raleigh, NC facility. Nitronex currently operates more than 11,000 square feet that includes: materials growth and characterization; a 100mm process line; in-house assembly; packaged test; and reliability test facilities. The facility has 1,000 square feet of cleanroom space for wafer fabrication, and is equipped to process 100mm wafers. The device-testing infrastructure includes: automated parametric DC testing; on-wafer RF power testing; packaged RF power testing; and a reliability

and burn-in station capable of operating up to 100 packaged parts at a time. Test results are collected into a database, allowing quick and convenient data analysis and correlation to be performed over an arbitrary number of wafer and process generations. This arrangement has enabled rapid development cycles and accelerated the rate of learning.

C. Baseline concept

As in any development environment, a significant level of engineering activity is constantly underway in order to meet performance and yield goals. A variety of methods are employed, including the use of design of experiments, split lots, and physical simulation. Additionally, at any given time, approximately 10%-20% of the capacity is dedicated to running lots of standardized process flow, which we refer to as baseline lots. All recipes, procedures, and tests associated with these lots are maintained under revision control. The process delivers a constant standard of devices for product development, reliability studies, and customer sampling. Baseline lots also serve to provide a relatively large body of data against which many experiments are assessed.

In order to control how baseline changes are adopted, a cross-functional revision control team meets regularly to initiate and review data from qualification events. Presently, a qualification event involves anywhere from 4 to 24 wafers and includes data collection through packaged testing. Seven major qualification events were initiated and five changes were adopted.

PROCESS TECHNOLOGY

A. Epitaxial Process

At Nitronex, GaN is epitaxially grown on 100-mm silicon <111> substrates using a custom-built, single-wafer MOCVD (Metal-Organic Chemical Vapor Deposition) system. The SIGANTIC™ process enables growth of GaN on silicon substrates overcoming the mismatch in lattice constant and coefficient of thermal expansion by the insertion of a stress mitigating transition layer. The current baseline structure is an undoped AlGaN/GaN HFET with a barrier layer comprised of 20% AlN mole fraction, resulting in typical carrier concentrations of approximately 6-7x10^{12}cm^{-2} and mobilities around 1300cm^2/Vs.

B. Device Fabrication

The baseline process flow is typical for GaN-based devices. This process is similar to other compound semiconductor FET technologies. Devices can be built with as few a six mask levels. All levels are performed by I-line stepper lithography, allowing for a fast and high yield fab turnaround. Ohmic contacts are comprised of Ti/Al/Ni/Au and formed by use of rapid thermal anneal (RTA). Device isolation is achieved by ion implantation. The gate is comprised of Au/Ni with a nominal length is 0.7µm. The surface of the semiconductor is passivated with a SiN dielectric layer, deposited by plasma enhanced chemical vapor deposition (PECVD). Finally, a 4µm gold airbridge interconnect level is formed by electroplating. Wafers are then thinned to 6 mils and the backsides metallized with Ti/Au to facilitate subsequent AuSi eutectic attach into standard ceramic power packages with CuW headers. Additional details of the device layer growth and fabrication have been reported elsewhere [5].

As an example of the baseline evolution, Figure 1 shows the progress of device efficiency with process generation. This progression has been achieved by optimization of the epitaxial process and specific unit processes.

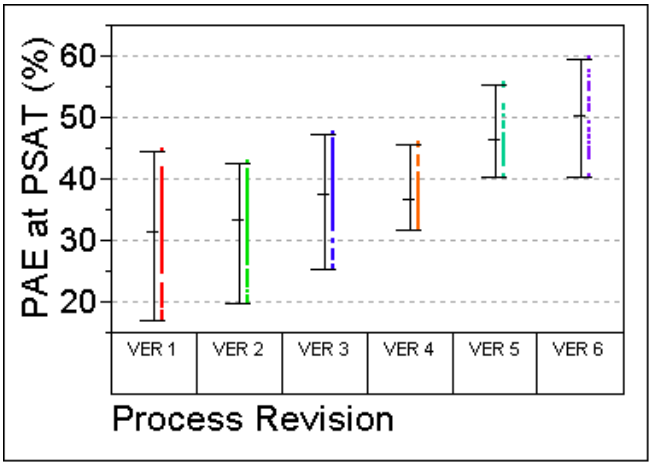

Fig. 1 Progression of power added efficiency across several process generations. Each bar includes entire population.

C. Typical process specifications – in line testing

In-line DC and RF characterization are performed at several test points throughout the process flow to assure wafer integrity and to ensure transistor performance within the baseline specification. In-line DC testing of the process control monitors (PCM) is performed on all wafers using a Keithley S400 Parametric Test System. The present baseline process exhibits I_{DMAX} = 630mA/mm. Three terminal off-state breakdown (BV_{DS}), defined as V_{DS} at which drain current exceeds 1mA/mm averages ~150V whereas off-state drain leakage (V_{GS} = -8V and V_{DS} = 100V) averages 0.15mA/mm. Contact resistance for the baseline process averages 0.75 Ω·mm. The uniformity of pinchoff voltage (V_P) for this process exhibits an intra-wafer variation ~325mV. On wafer load-pull at 2.14GHz is performed on five sites for all wafers using a Focus-Microwave Load-Pull System. Standard 2mm unit cells (200µm unit gate width), tested with an applied V_{DS} of 15V, exhibit saturated power densities (P_{SAT}) of ~1.3W/mm and associated drain efficiencies of ~50%.

D. On wafer product testing

Full DC screening of every wafer is performed for large periphery device (currently 16 and 36mm gate width) is performed using a FETtest 3600 ATE system. A suite of on-state and off-state parametric tests is performed at this test level. Figure 2 shows a typical wafer map generated from this data collected on 36mm devices.

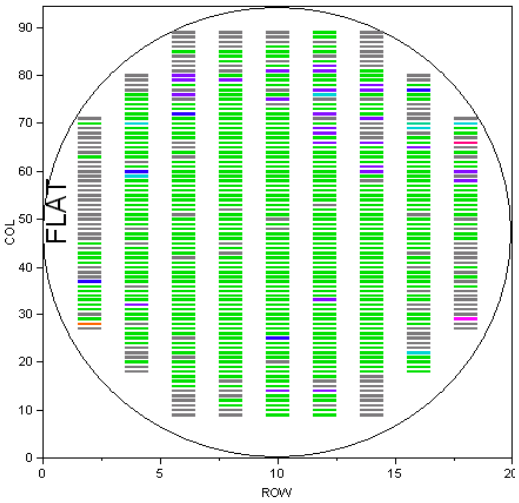

Fig. 2 FETtest wafer map of 36mm devices across a 100mm GaN-on-Si HFET wafer. Green die conform to Nitronex baseline performance specifications. For this wafer yield was 67% .

H. Reliability

Each wafer from the baseline production process is sampled for wafer acceptance testing that includes 24-hour high temperature operation life testing (HTOL). To date, over 1,500 devices from more than 150 wafers have been screened. Long-term HTOL testing projects that over a 20-year life, the present baseline devices exhibit ~4% degradation in DC parametrics such as Idss, Vp, and ~0.5dB reduction in saturated output power at a junction temperature of 200°C [6]. Additionally, infant mortality levels have remained consistently below 1%. Baseline devices have passed a battery of additional reliability tests. These include temperature cycle (-65/150°C over 250 cycles), autoclave (121°C, 15psi, and 96hrs), and Electro-Static Discharge (ESD) testing at 500 and 1000V. These results, represents a strong first confirmation of the basic reliability of III-Nitride on silicon technology.

RESULTS AND DISCUSSION

A. Challenges to epitaxial growth unique to this technology

Use of high-resistivity (HR) silicon substrates have been shown to provide an effective platform for the realization of RF circuitry. As an example, Reyes and co-workers [7] have shown the attenuation properties of coplanar waveguides fabricated on HR silicon to be similar to those fabricated on semi-insulating GaAs over a wide range of temperatures and bias. Substrates with resistivity >10,000Ω·cm at a reasonable cost are readily available. During growth care must be taken to avoid the undesirable diffusion of aluminum and gallium species into the silicon forming a p-type conductive layer. This conductive layer can result in parasitic losses that can adversely impact RF performance of circuit elements. Considerable effort has been made at Nitronex to develop a growth process that substantially reduces the formation of this parasitic layer. Physical measurements (SIMS and spreading resistance profiling) were used to quantify the reduction in parasitic conductivity. A notable improvement in the RF performance of the devices was also observed [8]. Figure 3 shows the resulting trend upward in power gain by baseline generation.

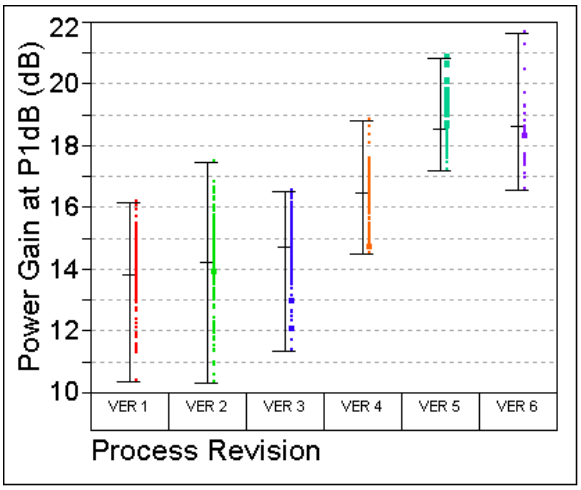

Fig. 3 Progression of power gain from on-wafer load pull measurements showing several generations of baseline process. Each bar represents the entire data set for the particular revision.

Substantial effort has also been spent on optimizing, material uniformity. The reactor design enables control of temperature and flow across multiple zones allowing for development of uniform processes. After minimizing temperature variation across the wafer during growth, designed experiments were conducted where the gas flow and gas composition were varied across the wafer. These experiments led to a set of process conditions where both layer thickness and alloy composition variation across the 100mm were minimized. Figure 4 is a trend chart for the AlN mole fraction of the device barrier layer across process and across wafer as determined by means of photoreflectance spectrometry. It is seen that after the first 6 runs, a process change was implemented in the reactor that resulted in dramatic improvement in AlN% variation across wafer. It should be noted that control of the barrier layer

composition is of considerable importance since the built-in field that induces a 2DEG, and hence controls the total charge, is linearly proportional to the AlN mole fraction in these structures.

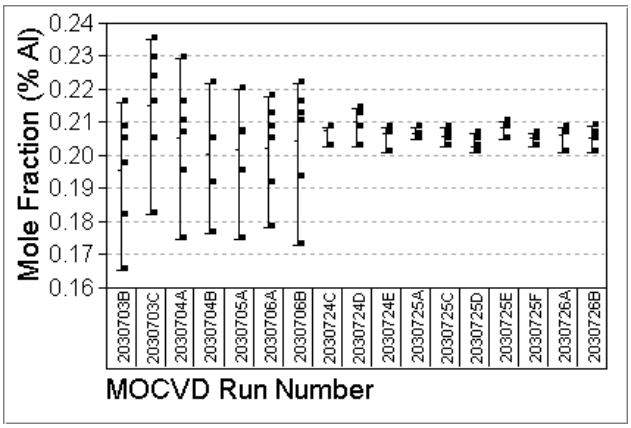

Fig. 4 Trend chart of AlN content in the barrier layer for over 18 repeat AlGaN/GaN HFET growth runs. The AlN mole fraction is given for 6 equidistant radial sites on each wafer.

B. RF Performance

The improvements made in each process generation are measured in terms of their effect on the RF performance of the technology. The improvement in gain with process generation is shown in figure 3 and has already been discussed. In addition, figure 1 shows a dramatic increase in PAE during on-wafer testing.

The final test performed at Nitronex is a WCDMA measurement on a large periphery packaged device. This test is designed to quantify the devices ability to address the needs of the W-CDMA base transceiver station output power stage. Recently we reported results in excess of 15W linear output power under W-CDMA modulation at 28V operation with and associated drain efficiency of 29% and –39dBc ACPR [6]. Newer process generations are already showing potential for improvement.

CONCLUSIONS

It has been shown that GaN-on-Si can meet the performance and reliability requirements of today's more demanding applications. Equally importance, the use of silicon substrates will insure the economical viability of the technology. Given the high power densities and breakdown voltages achievable with this technology, we expect it will prove enabling to many future applications. Nitronex further expects that with coming generations of process, performance levels will continue to increase.

ACKNOWLEDGEMENTS

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ACRONYMS

HFET: Hetero-junction Field Effect Transistor
HR Si: High Resistivity Silicon
W-CDMA: Wideband Code Division Multiple Access