Balanced AlGaN/GaN-HFET amplifier based on 111-Silicon substrate

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Keywords: GaN, Amplifier, Hybrid Integration

Abstract

In this work a modular low cost RF-amplifier system is presented, based on AlGaN/GaN-HFETs on 111-Si, hybrid integrated on PCB, consisting of single stage and balanced amplifier modules. 50 Ohm matching of the modules is realized with the use of commercial available SMD-components, allowing to cascade the individual modules. Depending on the setup of the system, either the total RF-output power or power gain is increased. This concept results in more efficient heat sinking because of the resulting small transistor size in contrast to other concepts [1]. The concept and a special mounting technique allows to use low cost heat sinks like copper, keeping the total module cost down. The RF-amplifier system is realized and tested at 2 GHz. Presently the frequency range is extended to 5 GHz.

INTRODUCTION

AlGaN/GaN high electron mobility transistors on SiC have shown their potential for being used in high power / high frequency amplifiers [3]. Nevertheless, commercializing these devices, the demand of cheap HFETs combined with low cost integration becomes very important. In this report a low cost RF-amplifier system consisting of individual amplifiers is presented. Depending on the setup, output power or power gain can be adjusted. The amplifier modules are fitted with AlGaN/GaN-HFETs grown and processed on 111-Si and hybrid integrated on PCB. With the use of discrete SMD-components 50 Ohm matching networks are realized on board, making the system flexible for the specific use. Increasing absolute output power two modules are connected parallel, while an increase in power gain is obtained by series connection. This concept based on distributed amplifiers, the effort for cooling is supported by the residual size of the individual transistor. Such a concept is only viable on low cost substrates like Si, where chip area is not yet of prime concern.

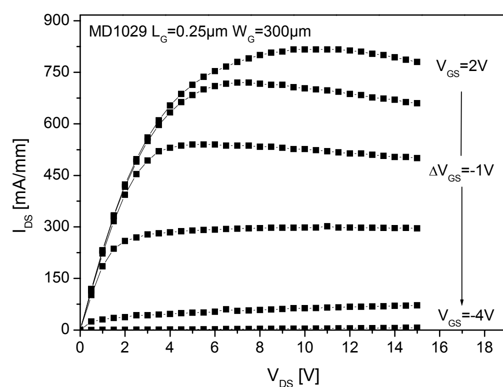

FIGURE 1
DC-OUTPUT CHARACTERSITIC OF ALGAN/GAN-HFET ON 111-SILICON.

ALGAN/GAN-HFETS ON 111-SILICON

The SiN passivated AlGaN/GaN heterostructures used are MOCVD grown on high resistive 111-Si. To reduce stress due to the different lattice constants of Si and GaN, a low temperature AlN-layer is used as nucleation layer and additional AlN strain relieve layers are introduced in the iron doped buffer [4]. The aluminum content of the AlGaN-cap layer is 28 %. A sheet charge density of $N_S = 8 \times 10^{12}$ cm^{-2} with a mobility of $\mu = 1170$ cm^2/Vs is measured by Hall effect at room temperature. Devices exhibit output current densities of $I_D = 820$ mA/mm with a gate length of $L_g = 0.25$ µm (fig. 1). On-wafer measurements yielded a cutoff frequency of $f_t = 31$ GHz and a maximum frequency of oscillation of $f_{max} = 27.5$ GHz for a 480 µm wide device at the bias point $V_{DS} = 15$ V and $V_{GS} = -1.5$ V. The f_{max} is still limited by the residual losses in the Si-substrate.
In class AB operation a CW drain voltage of $V_{DS} = 22$ V can be applied to the devices. Increasing V_{DS} self heating effects become dominant for large HFETs, resulting in constant output power and decreased power gain. Therefore the following investigations focuse on drain voltages of $V_{DS} = 15$ V.

INFLUENCE OF SEPARATION ON THE HFETS

The HFET devices are separated by dicing. After dicing, the maximum saturated output power is already decreased by 2 dB (V_{DS} = 15 V, V_{GS} = - 2.5 V, L_g = 0.25 µm, W_g = 240 µm, f = 2 GHz) (fig. 2). Further degradation in output power is seen with higher drain bias and also causing a drop of power gain. In addition, for diced FETs in class AB-operation the maximum CW drain bias needed to be reduced from V_{DS} = 22 V to V_{DS} = 18 V. No device instabilities [5] but self heating effects are made responsible for reduction in device RF-performance because pulsed RF-measurements with a period of 10 kHz and a pulse width of 10 µs before and after dicing yielded 27 dBm output power, equivalent to on-wafer CW measurements.

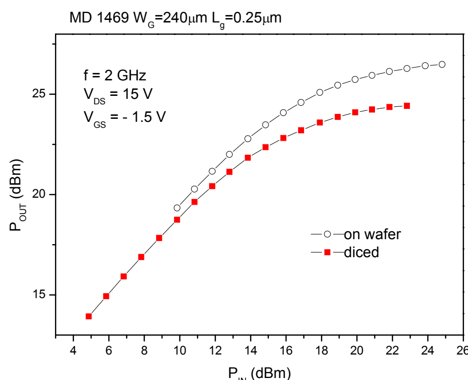

FIGURE 2
COMPARISON OF OUTPUT POWER: ON-WAFER AND DICED HFETS.

PACKAGING-MOUNTING TECHNIQUE

Amplifier modules are realized using micro strip lines on Ro 4003 material (PCB). Hybrid integration is accomplished by mounting the diced HFETs with a size of 0.8 x 0.8 mm^2 on a copper plate with silver glue (σ_{th} = 1.64 $Wm^{-1}K^{-1}$). The silicon substrate acting as heat spreader is efficient enough allowing to use high thermal conductive silver glue to mount the HFETs on the above mentioned copper plate. Connection between the HFETs and the PCB is established by gold wires, directly bonded onto the pads and the PCB. Matching networks designed for a dedicated frequency are realized using low cost discrete SMD components, calculated from on-wafer small signal measurements. The modules are fitted with separate RF- and DC-connectors, by the help of on board bias tees.
Two amplifier designs are realized, namely a single stage amplifier and a balanced amplifier module. A schematic overview on the single stage amplifier is given in fig. 3. Separate matching networks at the in- and output assure

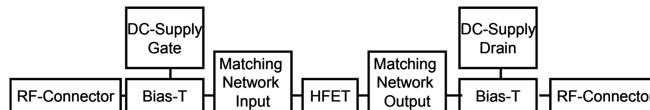

FIGURE 3
SCHEMATIC OF A SINGLE STAGE AMPLIFIER MODULE .

matching to 50 Ohm and also maximize power gain and RF-output power.

The balanced amplifier design, similar to the single stage amplifier design, is fitted with two 90° SMD hybrids. The advantage of the balanced configuration is a 50 Ohm input and output return loss regardless of the individual FET matching network. However, in this design a difference in output power between the FETs is eliminated, requiring two identical FETs for full output power. Beside the 90° hybrids, which are forcing in- and output to 50 Ohm, separate matching networks for each gate and drain are realized to obtain maximum gain of the amplifier module. Particular care has to be taken by realizing the matching networks. Due to high complexity, an increase in the length of the micro strip lines has to be taken into account in the design.

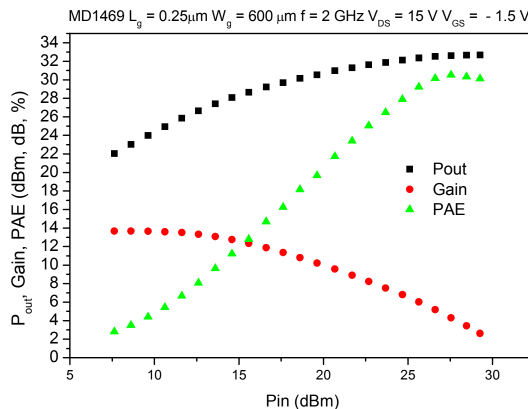

FIGURE 4
RF-POWER MEASUREMENT OF A SINGLE STAGE MODULE AT 2 GHZ .

AMPLIFIER RESULTS AT 2 GHZ

Single stage amplifier modules, operating at 2 GHz are realized using diced HFETs with a gate width of W_g = 600 µm and a gate length of L_g = 0.25 µm. Saturated RF-power measurements with these single stage modules yielded a linear gain of 13 dB with a maximum saturated output power P_{OUT} = 2 W equivalent to $P_{OUT,Norm}$ = 3.3 W/mm (V_{DS} = 15 V, V_{GS} = - 1.5 V), (fig. 4).

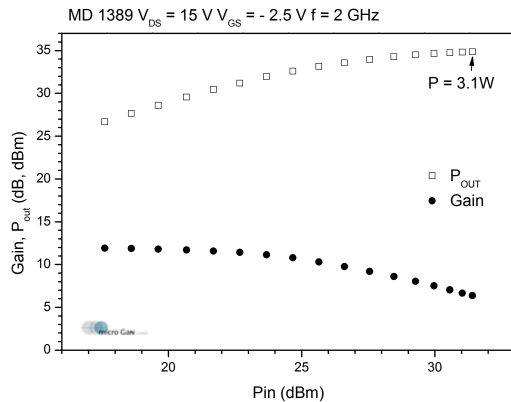

FIGURE 5
RF-POWER MEASUREMENT OF A BALANCED AMPLIFIER MODULE AT 2 GHZ WITH A MAXIMUM OUTPUT POWER OF 3.1W.

Balanced amplifier modules are realized, using two diced HFETs with a gate width of W_g = 2 x 1.5 mm and a gate length of L_g = 0.25 µm. Saturated RF-power measurements with these modules yielded a saturated output power of P_{OUT} = 3.1 W (V_{DS} = 15 V, V_{GS} = - 2.5 V, f = 2 GHz) and a linear gain of 12 dB (fig. 5).

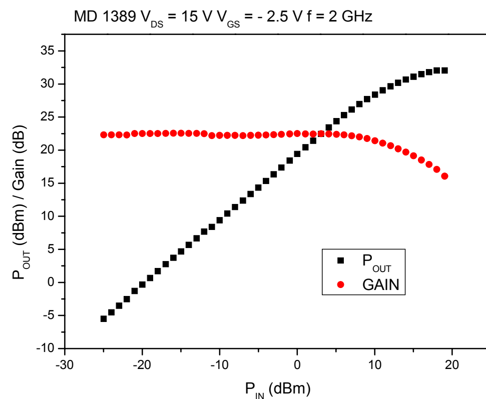

FIGURE 6
RF-POWER MEASUREMENT OF A SINGLE STAGE AMPLIFIER CONNECTED IN SERIES WITH A BALANCED AMPLIFIER MODULE AT 2 GHZ.

In order to increase linear gain, both modules, the single stage and the balanced amplifier are connected in series, where the single stage module is taken as preamplifier. In this configuration the linear gain increased by about 10 dB to 23 dB (fig. 6).

For a balanced amplifier module with W_g = 2 x 480 µm, a saturated output power of P_{out} = 1.8 W (equal to 1.9 W/mm) is obtained. A two-tone test at 1.9 GHz with a tone spacing of 1 MHz reveals an output-refered IP3 (OIP3) of 44 dBm. (fig. 6).

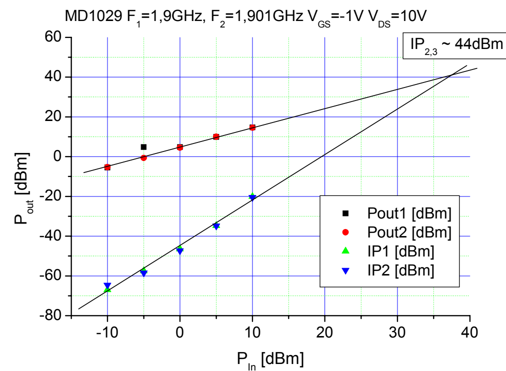

FIGURE 6
AN OIP3 +44 DBM IS OBTAINED FOR A BALANCED AMPLIFIER MODULE.

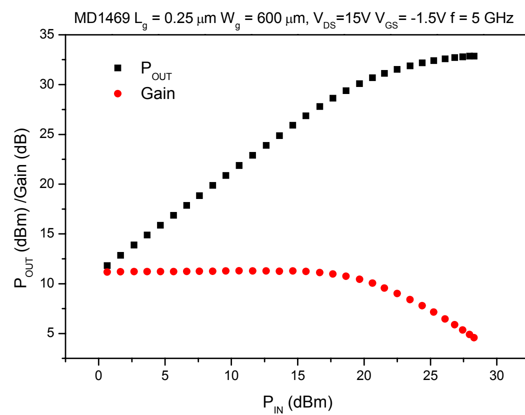

FIGURE 7
RF-POWER MEASUREMENT OF A SINGLE STAGE MODULE AT 5 GHZ.

AMPLIFIER RESULTS AT 5 GHZ

Similar to the 2 GHz modules, single stage amplifier modules operating at 5 GHz are realized using diced HFETs with a gate width of W_g = 600 µm and a gate length of L_g = 0.25 µm. Saturated RF-power measurements with these single stage modules yielded a maximum saturated output power P_{OUT} = 2 W equivalent to $P_{OUT,Norm}$ = 3.1 W/mm with reduced linear power gain of 11 dB (V_{DS} = 15 V, V_{GS} = - 1.5 V), (fig. 7). For decrease in power gain, an imperfect matched input is made responsible, because a necessary capacitance value for the matching network was not obtainable at the time.
Experimental balanced amplifier modules are under test.

CONCLUSION

A modular RF-amplifier system is presented using low cost amplifier modules based on AlGaN/GaN-HFETs on 111-Si. Hybrid integration on PCB as well as the use of commercial available discrete SMD components are major keys in the low cost realization. To employ a low cost glue-packaging technique has been possible due to the small active transistor size.

At 2 GHz with 50 Ohm matched in and output, a maximum saturated power density of 3.3 W/mm is obtained for a single stage amplifier module. A realized balanced amplifier module yielded 3.1 W absolute output power. By series connection of these amplifiers, the linear gain is increased to 23 dB.
First realized single stage modules with operating frequency at 5 GHz yielded 3.1 W/mm output power, indicating that the concept also is viable for higher frequencies.

ACKNOWLEDGEMENTS

The authors would like to thank M. Mammel and the other people from the printed circuit board facilities, University of Ulm, Ulm, Germany, for manufacturing PCBs, as well as Y. Men, University of Ulm, for supporting the submicrometer lithography.

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ACRONYMS

FET: Field Effect Transistor
HFET: Hetero Field Effect Transistor
PCB: Printed Circuit Board
V_{DS}: Drain-Source Bias
V_{GS}: Gate-Source Bias
W_G : Gate Width
L_G : Gate Length
AlGaN: Aluminium Gallium Nitride
AlN: Aluminium Nitride
SiC: Silicon Carbide