Multiple Level Plated Gold Interconnect for III-V Circuits

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Abstract

Performance for III-V circuits is increasingly constrained by the limitations of lift-off type interconnect metal schemes. Enhancements in device performance will require a silicon style interconnect process with shorter signal routing paths to take full advantage of these improvements.

INTRODUCTION

Northrop Grumman Space Technology has developed a modular four level plated gold interconnect process utilizing low k dielectrics (BCB)[1] allowing integration into numerous III-V processes; Including but not limited to: GaAs and InP HBT, GaAs and InP HEMT, and Sb based HBT technologies. (See Figure 1 for the schematic of the process). During the development of this interconnect system, numerous obstacles were encountered and overcome before a consistent high yielding production process was finally achieved. This paper will describe the design and development of the high yielding, plated gold, and low k dielectric interconnect process that is compatible with numerous NGST technologies.

PROCESS CONSOLIDATION

Currently NGST employs several different interconnect processes for the various III-V production technologies (See Table 1). Our main two drivers for creating a new interconnect process were process consolidation and circuit performance. Product integration and manufacturing ease often requires consolidation to one interconnect process. In addition, high density and high functionality circuits require narrower pitches to achieve the desired circuit performance. To achieve this, improvements to both the metal plating process and the seed layer etch are needed.

Initial design rules for the new process were established based upon available photo resist capabilities; need to enhance circuit performance, and repeatability and robustness requirements. To achieve these goals, improvements in nearly all facets of the interconnect process were necessary. The initial development included experiments for dielectric adhesion; dielectric etching for vias, dielectric etching for planarization, plated metal seed layer deposition, plated metal seed layer etching (wet vs. dry) and plated metal deposition.

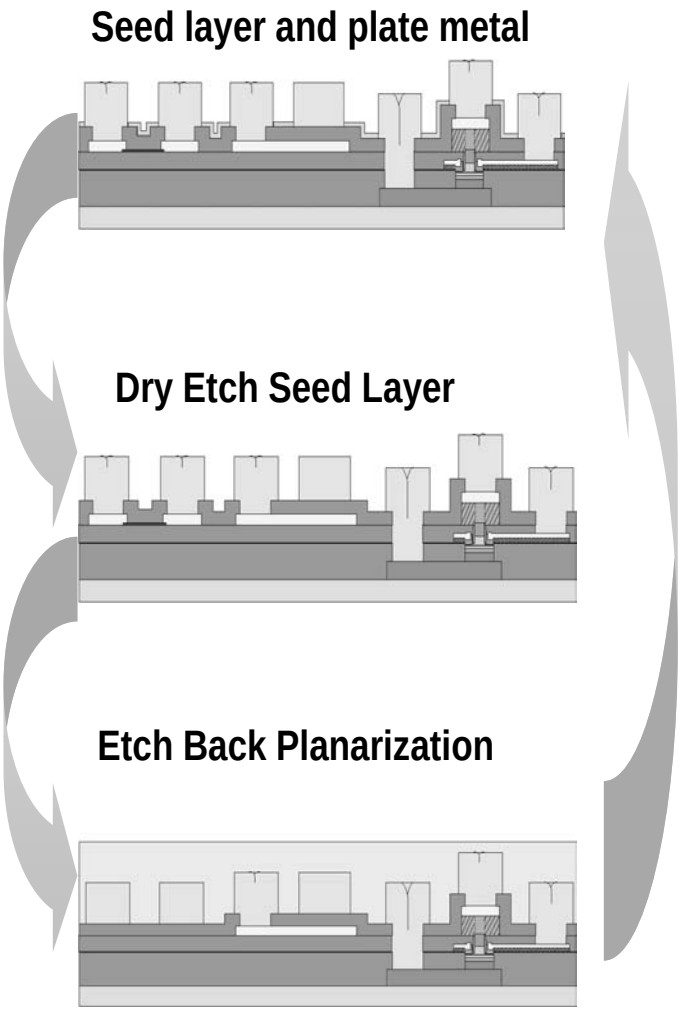

Figure 1. Process flow diagram for each metal and dielectric layer. These steps are repeated for each new metal layer.

Experimentation was at first limited to two levels of plated gold with a single low k dielectric layer in between the metals. It is, of course, the first layers of interconnect metal which require the tightest line size and via specifications. Subsequently, both a second level of dielectric and a third level of plated gold was introduced. From there, it was straightforward to implement the 4th layer of metal.

TABLE I
COMPARISON OF CURRENT INTERCONNECT PROCESSES WITH NEW PLATED GOLD INTERCONNECT PROCESS

	HEMT	**Microwave HBT**	**Digital HBT**	**New Interconnect**
Met 1	0.8 µm evaporated 3.25 µm pitch	0.8 µm evaporated 3.25 µm pitch	0.8 µm evaporated 3.25 µm pitch	1 µm thick plated 2 µm pitch
Met 2	4 µm plated 8 µm pitch	4 µm plated 8 µm pitch	2 µm evaporated 3.5 µm pitch	1 µm thick plated 2 µm pitch
Met 3	None	None	None	2 µm thick plated 4 µm pitch
Met 4	None	None	None	3.5 µm thick plated 6 µm pitch

EXPERIMENTAL

It is well known that BCB, when fully cured, does not adhere well to itself. Experiments to alleviate this condition, such as using partial curing, proved to be incompatible with via etch processes. A method was devised which solved the adhesion problem. Via etch processes also proved to be very problematic. We found that the photo resist mask used in the initial development could not produce fine enough geometries due to the low etch selectivity between the photo resist and BCB. We solved this problem by using a hard mask with higher etch selectivity properties. This however, presented another problem in that plated gold would not plate into small vertical walled vias. Further experimentation showed that a slightly tapered via could keep via geometry small enough and still allow plated gold to fill the tapered via. The multiple step via etch process was performed on a Trikon etcher using various combinations of SF6, CHF3, Oxygen and Argon so that both the BCB and the hard mask would be etched optimally (see figures 2 and 3). This process resulted in very high yields for our via chain test structures.

A new dry etch process to remove the seed layer metal was also developed and the gold plating process was improved to reduce the gold grain size. This allowed for finer geometries for the plated gold (see Figure 4). With these processes we are now able to fabricate one-micron thick plated metal with a two-micron pitch (see Table II). We are also able to plate Metal 1 onto HBT devices as well (see figure 5). We expect to decrease the pitch even more in the near future.

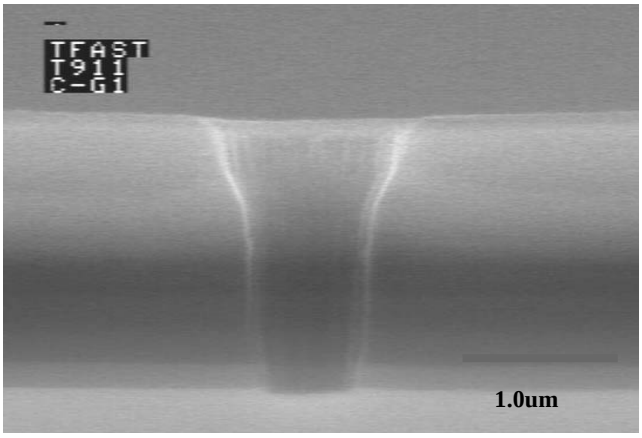

Figure 2. Tapered Via

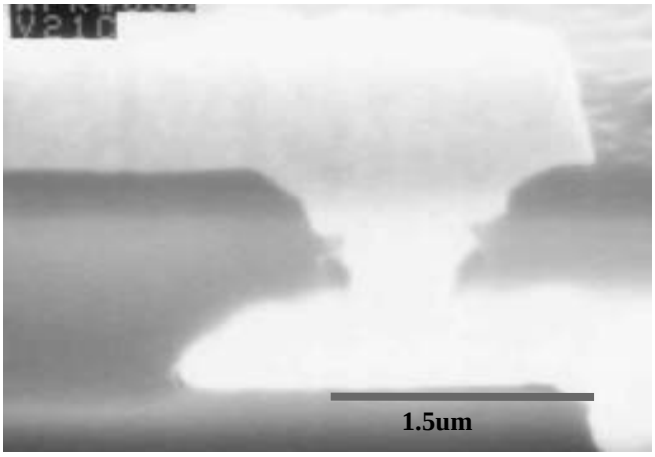

Figure 3. Plated MET 1 to MET 2 Via

TABLE II
YIELD PERCENTAGE OF 6 MILIMETER COMB STRUCTURES VS. PLATING CURRENT AND SEED LAYER ETCH PROCESS

Metal Width (um)	**SPACE (um)**	**WET/ 18mA**	**DRY/ 18mA**	**DRY/ 12mA**	**DRY/ 12mA**	**WET/ 12mA**
0.8	**1.2**	54.5	84.8	93.9	69.7	0.0
1.0	**1.0**	69.7	90.9	87.9	39.4	0.0
1.0	**1.4**	51.5	63.6	81.8	39.4	0.0
1.2	**1.2**	36.4	93.9	97.0	69.7	3.0
1.2	**1.6**	33.3	97.0	87.9	54.5	0.0
1.4	**1.4**	21.2	84.8	93.9	66.7	6.1
1.4	**1.6**	18.2	87.9	93.9	51.5	0.0

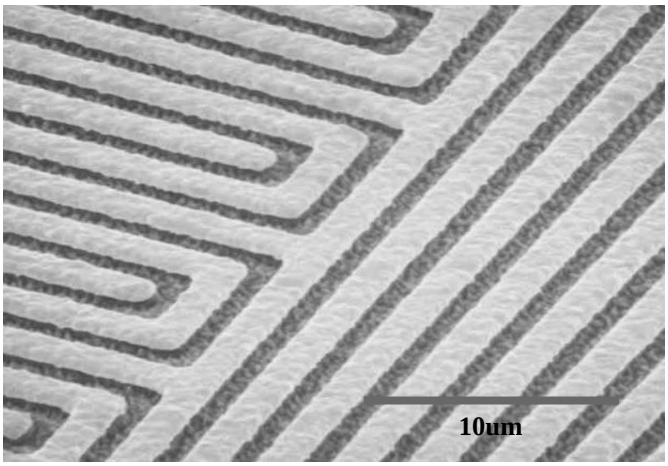

Figure 4. Plated MET 1

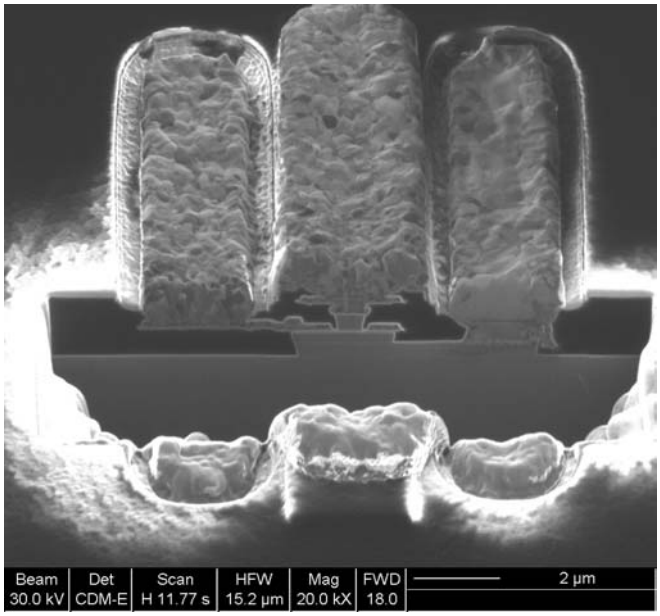

Figure 5. Plated MET 1 Contacting an HBT

CONCLUSIONS

In summary, Northrop Grumman Space Technology has been able to improve plated metal interconnect so that circuit density can be increased and electron transport time between devices can be decreased leading to better overall circuit performance.

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REFERENCES

[1] P.H. Townsend et al, ISHM Proceedings Oct. 1989.

ACRONYMS

HBT: Heterojunction Bipolar Transistor
HEMT: High Electron Mobility Transistor
BCB: Benzocyclobutane