A System for High Current Density Reliability Testing of HBT's with in-situ Measurement

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ABSTRACT

Space and other DoD systems require high reliability components, which will survive a long mission life. Heterojunction Bipolar Transistors (HBT's) are key components in these systems.

NGST has developed a robust system for long term testing of HBT's at very high current densities (200-300 kA/cm^2). This test measures current enhanced degradation that may not appear with standard high temperature reliability screening methods. The system is fully automated providing high current stress, with periodic comprehensive in-situ testing of all devices.

INTRODUCTION

Many space and DoD systems that use HBT components require extremely high reliability. Normal screening methods are not sufficient to test low activation, current accelerated degradation. Thus we developed a system for high current density screening of HBT's at a controlled temperature. This system tests for current enhanced failure mechanisms that standard high temperature reliability screening does not account for [1,2]. The system simultaneously stresses and individually tests up to twenty-four NPN HBT's.

HARDWARE

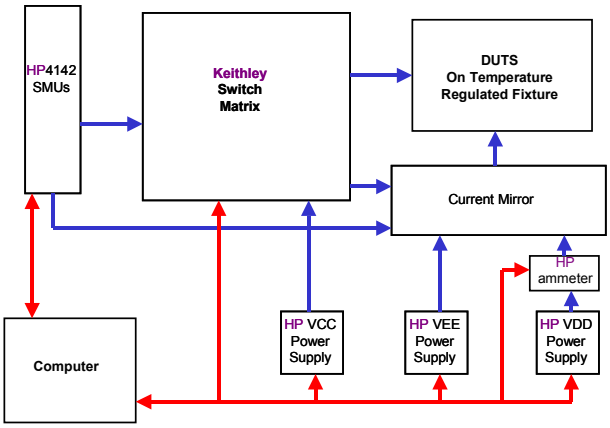

FIG. 1 - BLOCK DIAGRAM OF THE TEST SYSTEM

The system consists of two Keithley 707 switch matrices, an Agilent 4142 with 6 SMUs, three programmable power supplies, one current meter, one temperature meter, a Temptronic thermal chuck, a Northrop Grumman Space Technology (NGST) current mirror, a NGST fixture, a networked control computer, and a separate database server. The whole system is powered through a large uninterruptible power supply (UPS) so any brief power outages or fluctuations will not disturb the testing or damage parts.

FIG. 2 – THE TWO SWITCH MATRICIES, THREE POWER SUPPLIES, CURRENT METER, AND TEMPERATURE METER ARE ON THE TOP SHELF, THE THERMAL CHUCK CONTROLLER, TEST FIXTURE, CURRENT MIRRROR, AND SMU'S ARE ON THE BENCH TOP.

The test fixture is a hexagonal piece of gold anodized copper that sits on top of a thermally regulated chuck. On top of this there are six removable pie pieces that each contain a modified ZIF test socket with a large thermal shunt to the back of the DIP package. Each pie piece holds two 16 pin DIP headers. Each DIP header has space for two HBT devices.

The reliability calculations require a precise knowledge of the device temperature during the stress condition. Extensive thermal simulations of the fixture were conducted, along with precise measurements of actual temperature rise in the device [3].

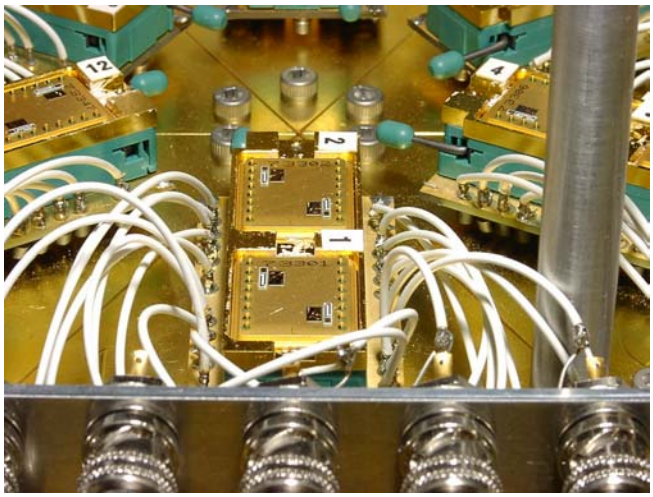

FIG. 3 – ONE PIE PIECE OF THE TEXT FIXTURE SHOWING TWO DIP HEADERS ON TOP OF THE THERMAL SHUNTED ZIF SOCKET. EACH DIP HEADER CARRIES A UNIQUE SERIAL NUMBER. THE TEG CHIPS WITH THE HBT'S ARE MOUNTED ON THE DIP HEADER NEXT TO A RRESISTOR NETWORK.

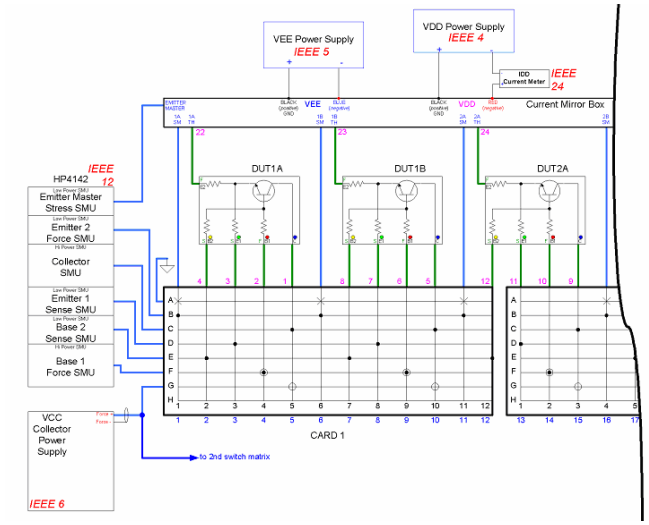

FIG. 4 – A PARTIAL CONNECTION DIAGRAM FOR THAT SHOWS HOW THE SWITCH MATRAICES CONNECT TO THE SMUS, DEVICES, CURRENT MIRROR, AND COLLECTOR POWER SUPPLY.

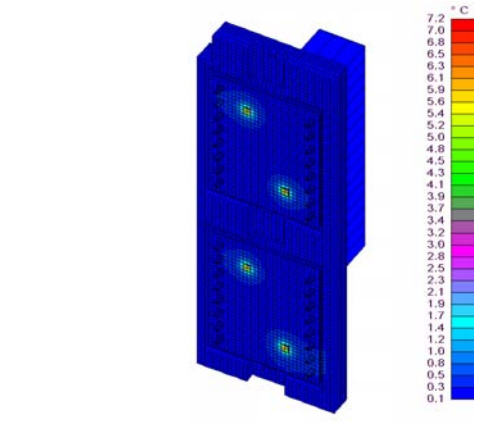

FIG. 5 – THREE DIMENSIONAL THERMAL SIMULATIONS SHOWING THE TEMPERATURE RISE IN THE ZIF SOCKET THERMAL SHUNT.

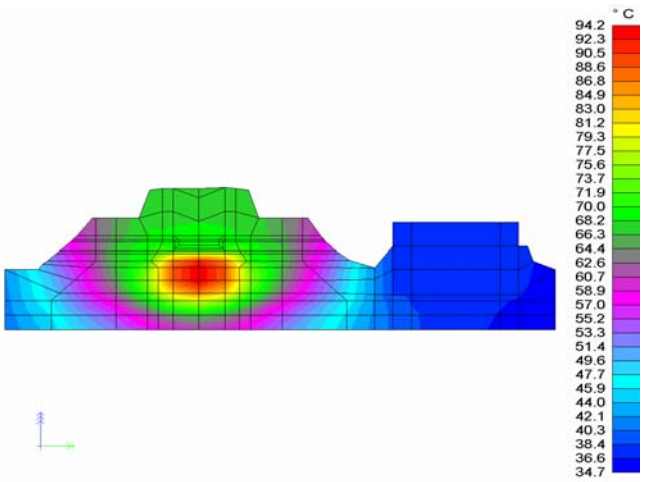

FIG. 6 – THREE DIMENSIONAL THERMAL SIMULATIONS SHOWING THE TEMPERATURE RISE OF A GAAS HBT ON A DIP HEADER IN THE ZIF SOCKET THERM SHUNT AND THE TRANSISTOR JUNCTION.

FIG. 7 – THE HEXAGANOL TEST FIXTURE WITH THE PROTECTION COVER OPENED TO REVEAL THE CONSTRUCTION. THE CURRENT MIRROR BOX CAN BE SEEN TO THE RIGHT

OPERATION

The system has four modes of operation; start up, stress, measure, and shut down.

During startup the operator enters the serial numbers of the parts into the system. The system then checks the database sever to see if this part has any prior test time on this or another system. If so it incorporates that data into the displayed test time.

Then during the second phase of start up, the system measures the emitter and base force resistors. These values are used during the stress period to measure the base and emitter currents of the device.

After startup the system enters a measurement cycle in which it measures a Gummel plot [$log(I_C)$ *and* $log(I_B)$ *vs.* V_{BE}] for each device by sequentially connecting SMUs to each. This data is written to the local hard drive.

Operation of the system is tied to a database, however the system is design such that the only time the system accesses the database is on start up when any history on the part being tested is retrieved. While the system is operating, it writes all data to the local hard drive. The database server then retrieves this data periodically. Thus during the inevitable network outages, the system continues to run and store data locally. Once the network is restored the database server can then again continue to retrieve data.

Programs on the database server generate daily status reports that include test time, DC current gain, and change in device beta.

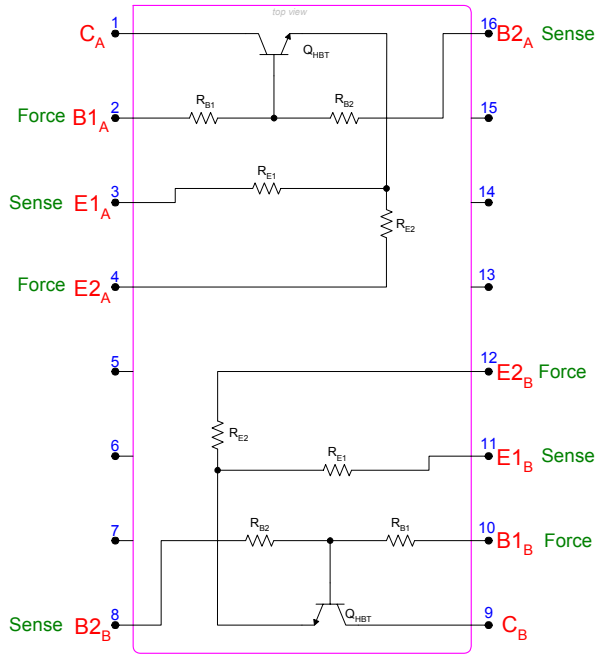

FIG. 8 – THE SCHEMATIC DIAGRAM OF HBT'S MOUNTED ON A DIP HEADER. THE RESITORS IN THE BASE AND EMITTER REDUCE THE PROCLIVITY OF THE HBT'S TO OSCILLATE. THE DUAL CONNECTIONS PROVIDE FOR KELVIN CONNECTIONS DURRING THE MEASUMENT SEQUENCE.

When the measurement cycle is complete the system enters the stress cycle in which all for the base force leads are grounded, all of the collectors are connected to the V_{CC} power supply, and each emitter is connected to a unique output of the current mirror. V_{CC} is then ramped up to it's stress value, and then the input to the current mirror is ramped up, which in turn ramps up all of the emitter currents to the stress value.

To avoid transients, no switching is done while the devices are under stress or being measured. Instead, only one device is completely monitored per stress cycle. The device being monitored is incremented after each measurement period and the cycle begins again.

After a preset stress cycle time the emitter currents and collector bias of all the devices are ramped down and a measurement cycle begins. The stress/measure cycles continue until the system is commanded to shut down by an operator, or if the temperature test fixture goes outside a preset window.

The shut down cycle first ramps down the power to the HBT's and then shorts all of the terminals to earth ground. The power to the current mirror is ramped down, and the notice of the system shutdown is sent to the operator via pager.

CONCLUSION

We have presented the design and operation of a fully automated system used for high current reliability testing at NGST. These systems have proven robust in operation and have been used continuously for the last two years.

REFERENCES

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[2] M. Wojtowicz, et al., "Analysis of GaAs HBT Reliability", 2003 GOMAC TECH Conference, April 3, 2003.

[3] P. C. Grossman, A. Gtierrez-Aitken, E. Kaneshiro, D. Sawdai, K. Sato, "*Characterization and Measurement of Non-linear Temperature Rise and Thermal Resistance in InP Heterojunction Bipolar Transistors*," IPRM. 14th Indium Phosphide and Related Materials Conference, 2002., 2002 , pp. 83-86

ACRONYMS

DIP: Dual Inline Package
HBT: Heterojunction Bipolar Transistor
NGST: Northrop Grumman Space Technology
NPN: a bipolar transistor with N type emitter and collector and a P type base
SMU: source-measure unit; can source or sink current, or can source voltage while measuring both.
TEG: test element group; a group of test structures and transistors placed on every wafer for process tracking and test.
UPS: Uninterruptible Power Supply
ZIF: Zero Insertion Force