Study of Reactive Ion Etching Process to Fabricate Reliable Via-Hole Ground Connections in GaAs MMICs

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Abstract

Via-hole etching process in GaAs has been studied using reactive ion etching with CCl_2F_2/CCl_4 chemistry. The effect of starting substrate surface, type of mask used and RIE process parameters viz. pressure and power on the surface morphology of etched wall and etch profile has been investigated. Extensive SEM characterization was carried out to study the surface morphology, etch depth and etch profiles. The starting polished surface with photoresist mask was found to give better surface morphology of the etched wall. The surface smoothness improved with increase in pressure but at the cost of anisotropy. Increase in power resulted in anisotropic etch profiles but with poor surface morphology. RIE process with 50 mTorr pressure and 200W power were found to give desired profile and acceptable surface smoothness. Finally these process parameters with photoresist mask and polished starting surface were implemented in MMIC via-process and MMICs with 50µm dia., 100µm deep, low resistance (~0.4Ω) via hole grounds were fabricated with yield > 80%. The inductance offered by these via's was ~ 25 ± 5 pH, well within acceptable limits.

INTRODUCTION

A backside via is an important element in GaAs MMICs. It provides electrically a low inductance grounding and at the same time serves as a heat sink. This step has proven to be one of the most difficult process associated with MMIC fabrication. It consists of via-hole etching and thin film metallization. Etching is performed from backside of the wafer to contact grounding pads on the front side[1-3]. Dry etching is preferred over wet etching because of its superior uniformity and dimensional control. The most common dry etching technique for etching via holes is reactive ion etching (RIE). High-density plasma etching techniques, such as electron cyclotron resonance (ECR) and inductively coupled plasma (ICP), have also been reported to give relatively higher etch rate and good anisotropy. Mainly chlorine based gases are used to etch III-V compounds and a number of chemistries have been reported including, BCl_3/Cl_2[4], $SiCl_4/Cl_2$[5] and CCl_2F_2[6]. Because via hole etching follows all other device fabrication processes, the process reliability and reproducibility are very important. The surface morphology and profile of the via are important not only for the inductance consideration but also for the success of backside metallization. The smooth morphology of the etched sidewalls provides reliable and good electrical contact with low resistance.

In this study we have investigated the effect of starting GaAs semi-insulating substrate surface (polished / unpolished), type of mask used (photoresist / Nickel) and RIE parameters (pressure and power) on the surface smoothness/morphology of the etched via-walls and resultant etch profiles with CCl_2F_2 / CCl_4 gas chemistry. The ultimate aim of the study has been to develop a reliable via-hole ground contact for MMICs upto 40GHz frequency range.

EXPERIMENTAL

Completely frontside processed, 650 µm thick, 3" GaAs wafers were coated with photoresist on front and mounted on sapphire carrier wafers with wax, frontside facing down. The backside of the wafers was thinned down to 100±5 µm thickness. Then via-hole pattern of 50 µm dia. holes were aligned and patterned using BSA lithography on the mounted wafer, either with 30 µm positive photoresist AZ9260 or 3000 A^0 of Ni. An oxygen plasma descum step prior to etching was utilized in order to remove any residual photoresist in the via hole which would contribute to the roughness of the etched surface.

Dry etching was performed in conventional parallel plate RIE. Wafers were placed on to the lower electrode to which 13.56MHz RF power was applied. The chamber was evacuated to a base pressure of 8e-6torr, by a turbomoleculer pump backed by a mechanical pump, before introducing the process gases into the chamber. The gas flow rates were regulated by mass flow controllers and chamber pressure was controlled by automatic throttle valve. The lower electrode temperature was kept at 30°C during the process to suppress the formation of less volatile compounds like GaF_3 [7]. One wafer was etched at a time. After etching, photoresist/Ni mask was removed and front to backside contact was made through etched hole by seed metal deposition (Ti/Pt/Au, 3000A°) using RF sputtering and gold electroplating (5µm). The surface morphology, etch depth and etch profile of etched hole were determined by cleaving through feature and examining under SEM.

RESULTS AND DISCUSSION

I. Effect of starting substrate surface:

Fig. 1 and fig. 2 show the SEM micrograph of etched surface (after 30 minutes of etching under identical conditions) of polished and unpolished starting substrate respectively at 5000X magnification. The starting polished surface of GaAs substrate leads to smooth morphology of the etched surface whereas the unpolished starting surface leads to rough etched surface with grass like structures and hence poor morphology. This has been attributed to more number of surface defects present on the unpolished surface giving rise to poor surface quality of etched area. It suggests that the defects on the surface play a major role in deciding the surface morphology of the etched surface. Rough morphology with grass like structures on unpolished surface indicates that the defective surface sites provide unequal etching sites causing uneven initial etching. The tip of the grass may be difficult to etch in an anisotropic etching condition. Thus the etching rate of tip is slower than the flat area and grass grows vertically as etching proceeds [8].

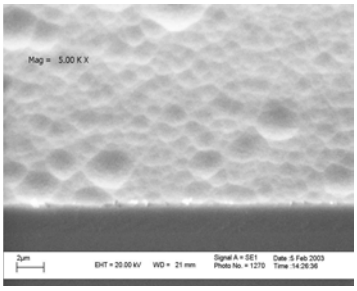


Fig.1. GaAs etched surface with polished starting surface.

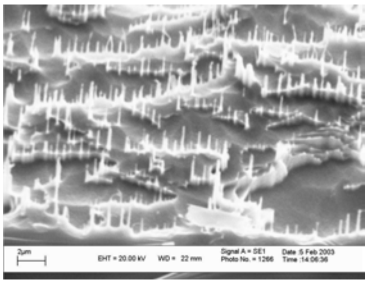
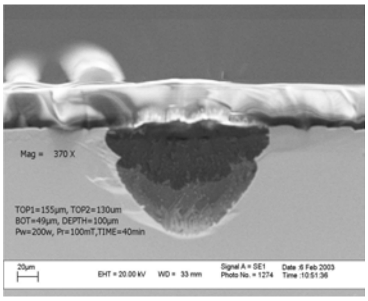


Fig.2. GaAs etched surface with unpolished starting surface.

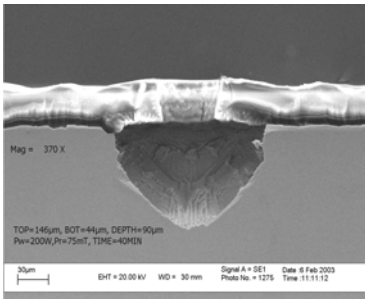
II. Effect of RIE process parameters:

Effect of power and pressure on surface morphology of etched via wall was studied at fixed flow rate ratio of 0.2 with photoresist mask. This CCl_4/CCl_2F_2 flow rate ratio was found suitable to obtain reasonably high etch rates, good surface morphology and anisotropic profiles[9].

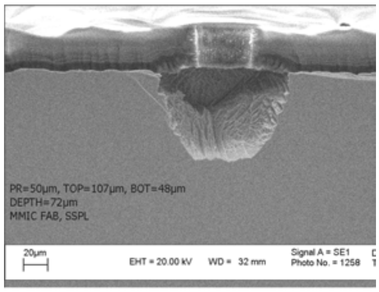
(i) Pressure: Figure 3(a), 3b) and 3(c) show the etch profiles obtained with photoresist mask, after 40 minutes of etching, for three different pressures i.e. at 100mTorr, 75mTorr and 50mtorr, respectively. And fig 4(a), 4(b) and 4(c) show the surface morphology of etched sidewalls at same magnification (1500X) for three different pressure readings. As seen from these SEM viewgraphs, the surface morphology is comparatively better at 100mTorr pressure but the profile obtained at 50mTorr pressure is suitable for subsequent step of metallization, to have better step



3(a) 100mTorr

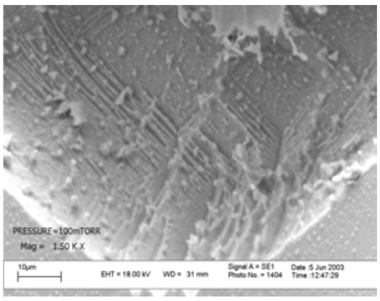


3(b) 75mTorr

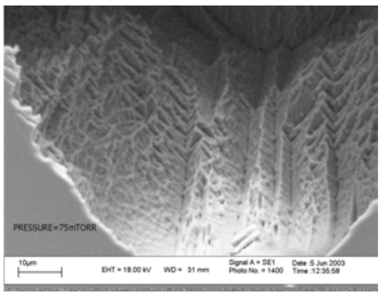


3(c) 50mTorr

Fig. 3. Etch profiles obtained at three different pressures (Power=200W, Flow ratio=0.2, Time=40min.)



4(a) 100mTorr



4(b) 75mTorr

4(c) 50mTorr

Fig. 4. Surface morphology of etched sidewalls at three different pressures (Power=200W, Flow ratio=0.2, Time=40min.)

coverage. This is due to the fact that at higher pressure, chemical component of etching dominates leading to smooth etched surface but the profile tends to be isotropic, leading to large undercut. At low-pressure, self-dc bias increases and hence physical component of etching increases, which promotes anisotropy but results in lower etch rate with slightly inferior surface morphology.

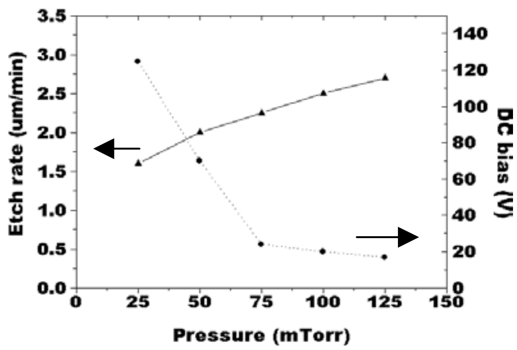


Fig. 5. Variation of etch rate and dc bias with pressure (Power=200W,Time=40min.)

Fig. 5 shows the variation of etch rate and dc self-bias with pressure, at power=200Wand etch time = 40min. The etch rate increases with pressure but dc bias reduces due to the increase in density of reactive species, which in turn reduces physical etching component. The dc self-bias value is very critical for good via profile, morphology and

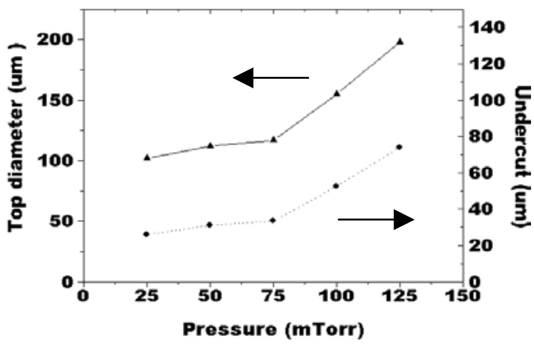


Fig. 6. Undercut obtained as a function of pressure (Power=200W, Time=40min.)

etch rate. It is a function of electrode material, chamber material and its geometry. Fig. 6 shows the top diameter of hole after etching, corresponding to 50 µm dia. hole opening in mask and undercut obtained with pressure. As pressure increases undercut increases due to increase in chemical etching component.

(ii) Power: Fig. 7 and fig. 8 shows the SEM viewgraphs showing surface morphology of via sidewall etched at power 200W and 250W, respectively with Ni mask under identical conditions (Pr=50mTorr, CCl_2F_2/CCl_4=0.2, Mag=1500X). It is clearly visible that with increase in power, etched surface morphology degrades due to increased self dc bias which in turn increases ion energy and hence surface roughness. But the etch profile at high power tends to be more anisotropic due increased physical etching component. At powers less than 200W although morphology was better but etch rate reduced with significant undercut, making etch profile unsuitable.

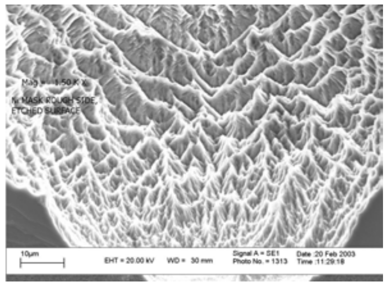


Fig. 7. The surface morphology of via sidewall etched at 200W (Pressure =50mTorr)

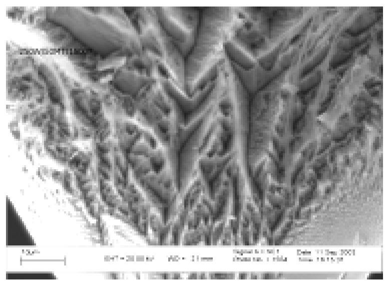


Fig. 8. The surface morphology of via sidewall etched at 250W (Pressure=50mTorr)

III. Effect of mask:

Fig 7 and fig.9 show the etched wall surface of via-hole with Ni mask and photoresist mask respectively at a magnification of 1500X, etched under identical conditions (Pr=50mTorr, Pw=200W, CCl_2F_2/CCl_4=0.2). As seen from these viewgraphs, via-hole etched with photoresist mask have resulted in smooth side walls and surface in comparison to the holes etched with Ni mask at same etching conditions (Pw = 200W, Pr=50mT, Time=75min). The photoresist mask provides better morphology of the etched side wall in comparison to the Ni mask, by passivating the sidewalls during etching. The photoresist from the mask gets sputtered and then gets re-deposited on

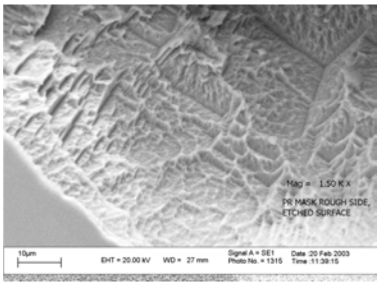


Fig. 9. The surface morphology of via sidewall etched at 200W with photoresist mask

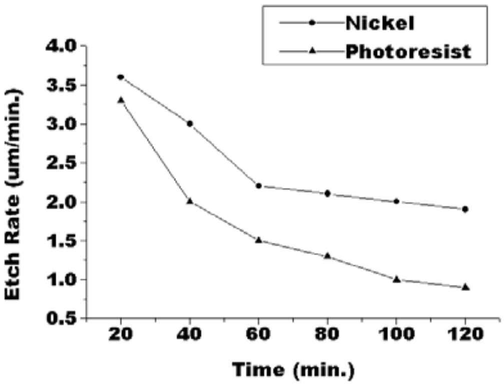


Fig.10. Etch rate variation with time

Table 1.
Optimized RIE process parameters

Etching mask	Photoresist
Starting surface	Polished
Power	200W
Pressure	50mTorr
Flow rates - CCl_2F_2 : CCl_4 :	35 sccm 7 sccm
Time	65min.
Etch rate	1.5 µm/min.
DC bias	70V

the sidewalls in the form of a polymer[10]. This polymer deposition promotes surface smoothness as well as anisotropy but reduces etch rate in comparison to Ni mask. Fig 10 shows the etch rate reduction with time for both the kind of masks at Pr=50 mTorr and Pw=200W. There is no such passivation in case of Ni mask and hence leads to rough etched surface with significantly higher etch rate. Thus the type of mask used, also plays significant role in deciding the surface quality of the etched surface as well as etch rate, apart from various RIE process parameters. Finally the photoresist mask with polished surface has been implemented in MMIC via-process and MMICs with 50µm dia., 100µm deep, good reliable low resistance (~0.4Ω) via contacts have been fabricated with yield > 80%. The optimized parameters for RIE process are shown in table 1. Fig. 11 shows the etch profile of a 100 µm deep via hole obtained under optimal RIE process parameters. The parasitic inductance offered by these via's was ~ 25 ± 5 pH, well within acceptable limits.

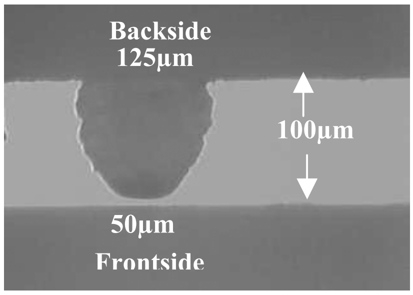


Fig. 11. Cross-section of dry etched, 100µm deep via hole

CONCLUSIONS

The surface morphology/roughness in backside via-hole etching is found to depend strongly on the surface condition affected by thinning process, RIE parameters and on the type of mask used. The wafers with unpolished back surface lead to rough morphology due to unequal etching of the surface, because of defects. Once these defects are removed by polishing after lapping, the etched surface becomes smooth free from any grass like structures. The surface smoothness improves with increase in pressure but at the cost of anisotropy. Increase in power results in anisotropic etch profiles but with poor surface morphology. The etch mask also plays significant role in deciding the morphology of the etched via sidewall surface. The photoresist mask provides better surface morphology in comparison to the Ni mask, by passivating the side walls during etching. Finally the photoresist mask with polished surface has been implemented in MMIC via-process and MMICs with good reliable low resistance (~0.4Ω) via contact have been fabricated with yield > 80%. The inductance offered by these via's was~25±5 pH.

REFERENCES

[1] R. A. Pucel, IEEE Trans., MTT-29, 513 (1981).

[2] L. A. D' Asaro et. al., IEEE Trans., ED-25, 5218 (1978).

[3] Y. W. Chen et. al., J. Vac. Sci. Technol., B 18(5), 2509 (2000).

[4] K. J. Nordheden et al., J. Vac. Sci. Technol., B 11(5),1879 (1993).

[5] S. Salimian et. al., J. Vac. Sci. Technol., B 5(6), 1606 (1987).

[6] A. E. Geissberger et al., J. Vac. Sci. Technol., A 3(3), 863 (1985).

[7] R. K. Klinger and J. E. Greene, J. Appl. Phys., 54, 1595 (1983).

[8] P. S. Nam et. al., J. Vac. Sci. Technol., B 18(6), 2780 (2000).

[9] D. S. Rawal et. al., J. Electrochem. Soc., 150(7), G395 (2003).

[10] S. J. Pearton et. al., J.Vac.Sci. Technol., B 11(2), 152 (1993).

ACRONYMS

MMIC: Monolithic Microwave Integrated Circuit
BSA : Back Side Alignment
RF : Radio Frequency
SEM : Scanning Electron Microscope