Gate Electrode Formation Process Optimization in a GaAs FET Device

Craig Carpenter, Chris Shepard, and Matt Stevenson

Skyworks Solutions, 20 Sylvan Rd. Woburn, Massachusetts, 01801
Tel: 781-376-3039 Email: craig.carpenter@skyworksinc.com

Keywords: Gate, CD, Resist, Liftoff, Solvent, Evaporator

Abstract:

This paper will describe how a gate electrode formation process in a GaAs FET device was analyzed and optimized for increased CD control and product throughput. Optimizations included a new resist in the photolithography process, a new solvent and equipment type in the metal liftoff process, and a new dome structure in the metal deposition process. These process optimizations resulted in a gate electrode formation process with improved CD control, a liftoff process with increased throughput, and the elimination of liftoff reworks.

INTRODUCTION

One of the most critical processes in building a GaAs FET transistor device is the formation of the gate electrode structure. The gate geometry discussed is on the order of 0.7µm. A properly functioning device must have excellent critical dimension control at this geometry and be defect free. At the same time the process must meet manufacturing standards of reproducibility and acceptable throughput. In order to achieve these goals at Skyworks Solutions the entire gate formation process was analyzed and optimized. It will be shown that a gate formation process was developed with improved critical dimension control and throughput.

The legacy gate formation process consisted of photolithography using JSRNR16 resist, metal evaporation over the entire surface of the wafer, and a manual bath type liftoff process using diethylene glycol n-butyl ether based solvent. The primary problems associated with the legacy process are poor CD control and low throughput. Other problems included poor liftoff characteristics resulting in excess metal and residues, and defects caused by scratches due to manual handling. These problems were analyzed and a series of process optimizations were performed.

LEGACY PROCESS DETAILS

The photolithography process consisted of JSRNR16 resist coated to a thickness of approximately 1µm on a TEL Mark VZ coater and exposed on an ASML 100 I-Line stepper.

The deposition process consisted of metal evaporation in a Temescal FCE2700 evaporation system with a 42-inch source-to-substrate throw distance. The Temescal system is a non-loadlock system capable of processing 24 wafers per run. The wafers are manually loaded onto a dome within the system. A metal stack of Ti/Pd/Au is used at a total thickness of 6000Å.

The liftoff process consisted of a manual immersion in a bath of diethylene glycol n-butyl ether based solvent at 90° C, an intermediate rinse in a DIW cascade bath, and a final rinse in an IPA bath. The diethylene glycol n-butyl ether based solvent performed the liftoff process and immersion times varied between 2 to 4 hours. After the final IPA rinse the wafers were individually and manually dried.

PROCESS PROBLEMS

The major process problems associated with the gate formation process were poor CD control and poor throughput. Other problems include residue, damage, contamination, and excess metal.

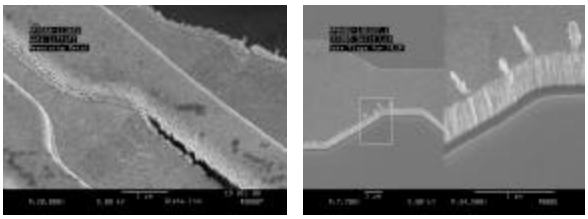
Control of the photolithography process is important to ensure proper CD and resist profile. The gate CD has a direct correlation to the device's electrical performance [1]. Each device is designed and tuned to operate with a gate of a specific length. Variations in length in either direction will result in a degradation of device performance. The resist profile is critical to the liftoff process [2]. A negative or re-entrant taper is required to have a clean metal liftoff. As the profile becomes less re-entrant liftoff problems will result. The photolithography process is optimized to print a gate with a specific length and resist profile.

The reasons behind the poor CD control were attributed to the 0.7µm geometry pushing the limits of the JSRNR16 resist. The JSRNR16 resist worked fine for the larger geometries that were being used when it was first introduced at this facility but at the current geometry of 0.7µm the JSRNR16 resist did not provide enough process latitude, especially in terms of sensitivities to hotplate temperature.

Problems with the throughput were mostly due to the liftoff process. The liftoff times varied between 2 to 4 hours resulting in low and unpredictable cycle times. Additionally lots would often have areas where various amounts of metal would not liftoff. These lots would then be subjected to a variety of reworks that further decreased the throughput by adding a minimum of 2 additional hours of processing time.

When a wafer did require a rework the metal lines were often damaged, Figure 1.

FIGURE 1
Gate Liftoff Problems



Metal Ripping Metal Flagging

Several reasons were attributed to causing the remaining metal problems. One was poor resist profile attributed to the photolithography process. As the resist profile becomes less re-entrant the area for solvent penetration becomes smaller. The liftoff becomes less effective when there is less solvent penetration. Another reason was the weakness of the solvent. A more aggressive solvent would strip resist faster and more effectively thus overcoming marginal profile situations.

There was also a problem of the metal flagging at the edge of the wafer. During the photolithography process an EBR process is performed by applying a solvent to the back of the wafer and allowing it to wrap around, approximately 1mm, to the front side of the wafer. This process removes unwanted resist thereby reducing contamination. However exposed GaAs is left on the front side of the wafer in the areas where resist is removed and during the metal deposition process the metal becomes tacked down in these exposed areas. After the liftoff process the tacked down metal leaves a macroscopic defect, referred to as edge flags, along the perimeter of the wafer.

To remove the edge flags they are scrubbed with a solvent soaked Q-tip. Problems resulting from this rework method include residue and particles from Q-tip and damage due to scratches to nearby devices.

PROCESS OPTIMIZATIONS

In the photolithography process a resist with improved process latitude at the 0.7µm geometry was evaluated. AZNLOF5510 was chosen as the new resist with the best process latitude. Table 1 shows some of the most significant process variables. A more robust process using the AZNLOF5510 was developed based on DOE results.

TABLE 1
Resist process latitude comparison

Process Parameter	JSRNR16	AZNLOF5510
DOF @ 0.5µm	0.5µm	1.0µm
DOF @ 0.7µm	1.4µm	1.8µm
PEB Sensitivity	75nm/°C	3.9nm/°C
Exposure Sensitivity	7nm/mj	2.5nm/mj
Develop Temperature Sensitivity	10nm/°C	4nm/°C

In the metal liftoff processes changes were made in both the types of solvent and equipment used. A more aggressive solvent, it terms of stripping resist, would be able to overcome some variations in resist profile, providing the liftoff process with more process latitude. Two NMP based solvents were evaluated and Table 2 indicates that both solvents give superior liftoff results.

EKC865 was chosen for the production process over Solvent A for two reasons. One, EKC865 was used in another Skyworks facility with reliable results. Two, an excellent working relationship was developed between Skyworks and EKC Technologies.

TABLE 2
Solvent Evaluation Summary

	Standard	Solvent A	EKC865
Composition	Diethylene glycol n-butyl ether 2-(2-aminoethoxy) ethanol Butyrolactone	N-methyl Pyrrolidone 100%	N-methyl Pyrrolidone N-(2-hydroxyethl)-2-pyrrolidone
L/O Time	120 Minutes	15 Minutes	15 Minutes
L/O Rinse	No residue	No residue	No residue

Yield and electrical data from several split lots was used to qualify EKC865. A summary is seen in Table 3.

TABLE 3
EKC865 Qualification results

Lot	Condition	Ig	Vbgd	%Yield
1	EKC865	-4.65	17.73	97.74
1	Standard	-3.35	20.26	94.49
2	EKC865	-10.13	14.51	85.7
2	Standard	-10.23	15.27	83.23

The last optimization to be made to the liftoff process was to convert it to a piece of automatic equipment. The gate liftoff process was the only liftoff process performed in a hood. All other liftoff processes were performed in a Semitool SST system. The major roadblock to moving the gate liftoff process to a SST system was the metal flagging seen at the edge of the wafer. It was not desirable to have the liftoff process fully automatic only to have to manually remove metal from the edges of the wafer. To eliminate the metal flagging problem modifications were made to the metal deposition process.

The metal flags at the edge of the wafer were due to metal being deposited directly on GaAs at the edge of the wafer in areas where the resist had been removed due to the EBR process. It was not desirable to alter the EBR process therefore the solution focused on not depositing metal in this area.

To control where metal was deposited, modifications were required in the dome structure of the Temescal evaporation system. It was desired to create an exclusion zone, an area where no metal was deposited, at the perimeter of the wafer

that would be larger than the area where the EBR had removed resist, yet smaller than the largest exclusion zone of the remaining processes. The MBE process created the largest exclusion zone of 2.8mm. If the exclusion zone for the metal deposition process was held under 2.8mm, MBE would remain the gating yield factor for edge die and there would be no yield loss due to the deposition exclusion zone.

The width of the evaporation exclusion zone is controlled by the size and alignment of the through hole in the dome where the wafer is held during deposition. The size of this hole was decreased from 98mm to 95mm and material was added at the wafer flat to protect the character window. More importantly, the wafer recess diameter was reduced to 100.33mm and a flat was added perpendicular to the dome centerline. This assured precise wafer alignment, while allowing SEMI STD maximum diameter wafers to be loaded and unloaded easily. The end result was a consistent 2.7mm exclusion zone at the perimeter of the wafer.

After the design was tested and refined, using an in-house manufactured test jig, a prototype dome was built to our specifications, by Temescal. Qualification of the new dome consisted of measuring gate offset at various positions within the wafer and across the dome. Gate offset is defined by where the gate metal is positioned within its recess. This offset is due to changing angle of incidence, relative to wafer position in the dome and site position on the wafer. The results of the offset measurements for qualification lots can be seen in Table 5.

TABLE 4
Offset data
Outer Position

Dome	Top	Left	Center	Right	Flat
Old	-.0021	-.01875	-.00205	.00835	-.0021
New	-.0025	-.01875	-.083	.02085	-.00205

Inner Position

Dome	Top	Left	Center	Right	Flat
Old	.0021	-.01045	.0021	.01875	.00415
New	0	-.0104	.00205	.0146	.00205

The differences in offset between the old and new domes were found to be similar. Wafers deposited with the new dome had a larger edge exclusion zone and after liftoff no metal flagging was seen at the edge of the wafer. The dome modifications were effective in eliminating the metal flagging problem. The new dome structure was released to production.

With the elimination of the wafer-edge metal flagging a process was developed on the SST system and qualified via production split lots. The results of the qualification can be seen in Table 5.

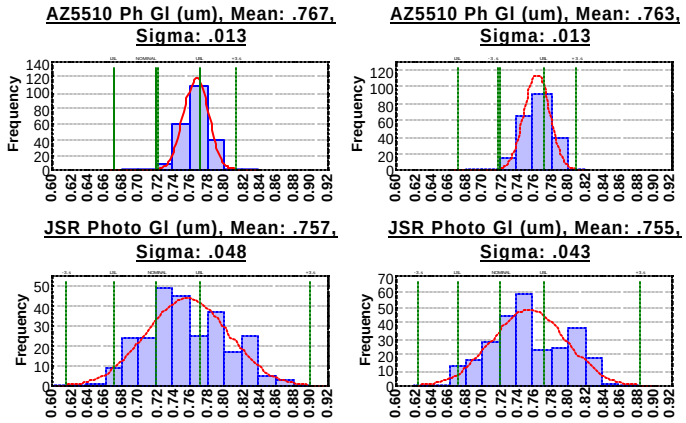
TABLE 5
Semitool SST system Qualification results

Lot	Tool	Vbgd	%Yield
1	Hood	17.54	87.3
1	SST	16.71	90.4
2	Hood	19.53	93.0
2	SST	18.22	88.0
3	Hood	21.91	95.8
3	SST	21.33	95.4
4	Hood	21.82	94.3
4	SST	20.82	93.0

RESULTS

Changing the resist to AZ5510 with an optimized process resulted in better CD control. Figure 2 shows a 64% reduction in the standard deviation of gate length for the AZ5510 resist when compared to JSRNR16. The data shows that targeting is at the upper end of the spec limit. This is to match the conditions of the JSRNR16 material. However the AZ5510 has more process latitude such that the CD can be lowered in the future if needed. The JSRNR16 resist was at its limit and could not go below 0.7µm.

FIGURE 2
Within wafer Gate Photo CD data

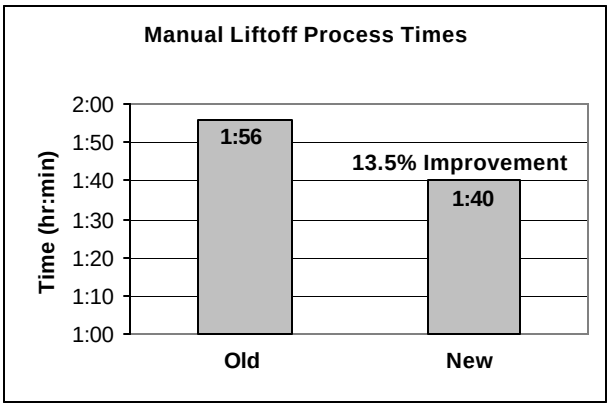


A throughput improvement was seen in the liftoff process. Due to better photo process control the resist profile was more consistent resulting in less metal remaining in the interior of the wafer after liftoff. The more robust solvent easily handled the smaller variations that were still present in the photo process. Modifications to the Temescal dome eliminated metal flagging at the edge of the wafers. These process optimizations combined resulted in the elimination of post liftoff excess metal issues. Figure 3 displays production data showing a 13% throughput improvement through the manual liftoff process.

Production data is not yet available for the automatic liftoff process. However, since it is an automatic process a process time of 27 minutes is a set value. This results in a 73% improvement over the optimized manual liftoff process and a

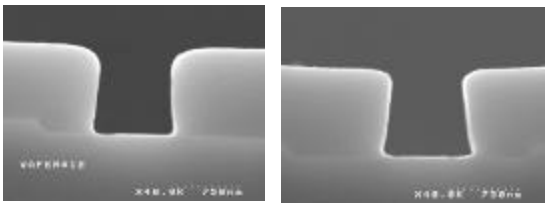
total improvement of 77% over the un-optimized liftoff process

FIGURE 3
Liftoff throughput improvement chart



There were additional benefits beyond the main goals of better CD control and increased throughput. Using the AZ5510 resist the proper resist CD and profile were achieved using a single versus double puddle develop dispense and shorter bake times, both soft and PEB, when compared to JSRNR16 conditions, Figure 4. Overall a 50% reduction in developer usage and a 90 second/wafer reduction in the coat/develop process were seen.

FIGURE 4
Gate photo resist profiles



JSRNR16 AZ5510

The liftoff process problems of excess metal, scratches, residues, and contamination were eliminated after changing the solvent and moving the process to an automatic system. Additionally the move to an automatic system results in a safer process for the operator by eliminating the exposure to hot EKC865.

While developing the new dome for the evaporation system work was done with the testing group to make sure that only die within the evaporation exclusion ring would get tested. This resulted is a reduction in test time by not testing known bad die.

CONCLUSION

This paper has shown how the gate formation process was analyzed and each step in the process optimized to result in a process with better CD control and a better product throughput. The process changes included using a new resist in the photolithography process, a new solvent in the liftoff process, changing to an automatic piece of equipment in the liftoff process, and re-engineering the metal evaporation system dome. The results of these changes were a decrease in CD variation of 64% with wider process latitude and an increase in throughput of 77% through the liftoff process.

An important point to note is the process changes made represent a cross-functional approach to the gate formation process optimization. Several different engineering groups were involved in this project and benefits seen in one area were often the results in changes from another area. The total gate formation process optimization could not have happened if it were not for the teamwork and cooperation between several groups.

ACKNOWLEDGEMENTS

The author would like to acknowledge Sarah Woolsey for help in the optimizations of the metal liftoff process, Aida Castro for help in the optimizations of the photolithography process, and Edward McCusker for help in building the prototype for the modification of the Temescal dome.

REFERENCES

[1] R. Williams, *Modern GaAs Processing Methods*, pages 58 – 65, 1990

[2] P. Van Zant, *Microchip Fabrication*, pages 313 – 314, 4th Edition

ACRONYMS

FET: Field Effect Transistor
CD: Critical Dimension
DIW: De-ionized Water
IPA: Isopropyl Alcohol
EBR: Edge Bead Removal
DOE: Design of Experiment
DOF: Depth of Field
PEB: Post Exposure Bake
NMP: N-methyl Pyrrolidone
SST: Solvent Spray Tool
MBE: Molecular Beam Epitaxy
GL: Gate Length