InGaP HBT Technology Optimization for Next Generation High Performance Cellular Handset Power Amplifiers

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Abstract

This paper reports on our new HBT technology developed for GSM, CDMA and WLAN PA application. The improvements are achieved by epitaxial, process and layout optimization. The device performance of the new technologies are presented and compared with our current available technology. The new device is able to survive VSWR 12:1 under 5V V_{CE} bias, and by tuning the power cell for maximum efficiency, we are able to achieve up to 67% PAE.

INTRODUCTION

GaAs based HBT is by far the most proliferated technology used in wireless communication applications such as cellular handset and WLAN power amplifier, mixer and VCO. Based on each individual application, unique stringent requirement on device performance such as ruggedness, power performance, stability, linearity and chip size reduction is being put forward. Optimization of device performance poses a significant challenge, as improvement in a parameter is most likely met with an adverse trade-off in another. However, with proper design and optimization, device performances could still be improved without imposing significant compromises. In this paper, we introduce a new generation of HBT technologies developed in WIN Semiconductors with momentous improvement in targeted parameters such as size reduction, ruggedness and linearity performance while other device performances remain applaudable.

DESIGN IMPROVEMENT

WIN currently offers two kinds of HBT technologies, namely, our H02U-00 (15V BV_{CEO}) process, aim at high linearity application (CDMA, WLAN), and H02U-10 (20V BV_{CEO}) process, aim at high ruggedness application (GSM). In our new line of technology introductions, generically termed HBT3 technology, we are able to provide better ruggedness and linearity performance without sacrificing in the power performance.

Epitaxial design is divided into two structures, one targeting ruggedness application, while the other targets high linearity application. Epitaxial structure design optimizations were done to i) improve linearity performance of the device (for CDMA application), ii) improve the transistor on-state breakdown, which could be monitored through the safe operating area (SOA), to achieve greater robustness (for both GSM and CDMA applications), and iii) increase device power efficiency by reducing the emitter resistance and thermal resistance.

Figure 1 shows the SOA region for the various epitaxial structure designs for GSM purposes. The improvement in SOA is mainly due to the optimization in collector structure [1]. As can be seen, by changing the collector layer design, we are able to alter the on-state breakdown of the device notably. Various designs are tested and fabricated, and upon process completion of the test structures, we measure the SOA and subject all designs to on-board ruggedness test. The best performance structure was then selected for our new technology offering.

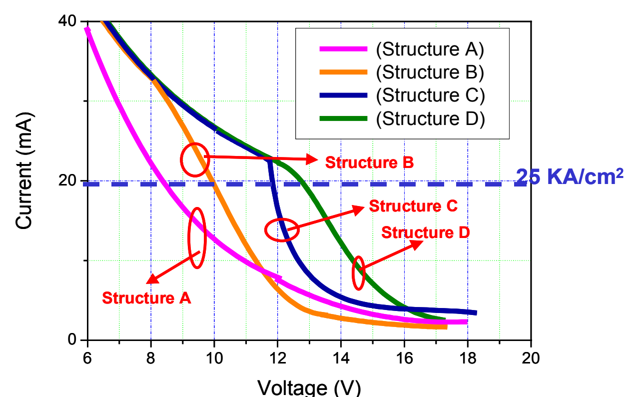


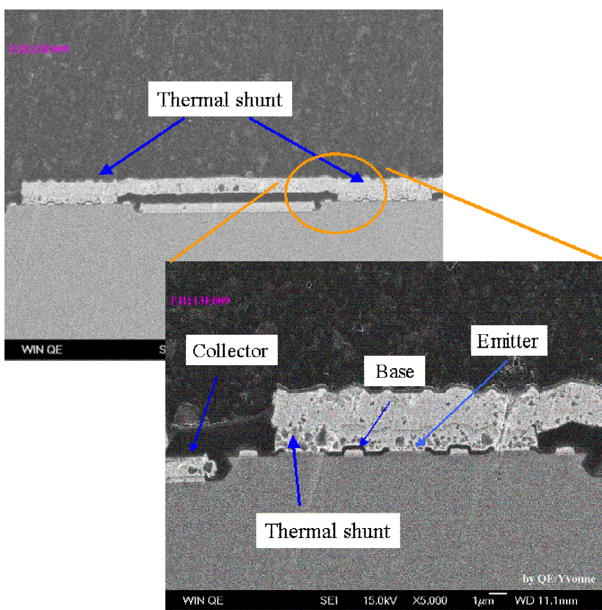
Figure 1. SOA performance for various GSM HBT3 epitaxial structures (80μm^2 emitter device).

The emitter resistance of an 80μm^2 transistor is reduced to 0.7Ω as compared to 1.5Ω in our H02U-00 and H02U-10 process. The resistance improvement is done by layer doping and thickness optimization in the emitter design.

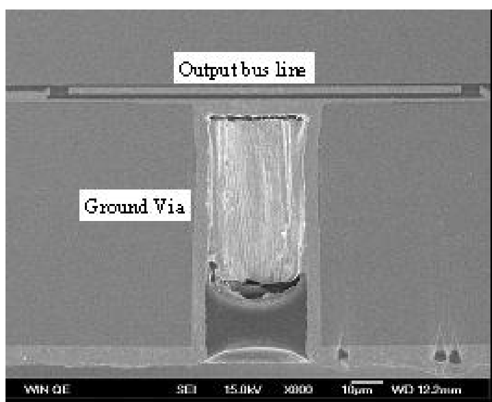
This improvement aids to maintain the power performance of the device while the ruggedness improves.

PROCESS IMPROVEMENT

In terms of process improvements, MIM capacitor dielectric thickness has been reduced, providing stack capacitors with unit capacitance of 900pF/mm^2 as compared to 450pF/mm^2 from our previous technology. New improved cell layout design coupled with smaller capacitors offer an area reduction of more than 20%. Improved metal scheme, layout and wafer thickness have also been employed to improve device thermal dissipation.



(a)



(b)

Figure 2. Cross section view of HBT3 devices indicating (a) Thermal shunts connecting emitter contacts and (b) ground via for improve thermal dissipation.

Figure 2 shows the cross section view of the devices from our new HBT3 technology. As the emitter region generates most of the heat during device operation, it is desirable to provide a most efficient way to dissipate the heat. As can be seen from Figure 2(a) and 2(b), all emitter fingers are connected through thermal shunts, and are connected to a ground via in a shortest possible route. Such layout scheme is successful in improving device thermal dissipation and improves its power performance.

Various metal layout schemes were also studied to further improve the device heat dissipation. The aim of the layout optimization is to have the heat source connected to as large metal area as possible. Four layout schemes were proposed. Figure 3 shows the SOA region measured from a same unit cell design with the 4 different metal schemes. From the results, we see that just by optimizing the metal layout, we are able to improve the device thermal resistance, and consequently the SOA region, rather significantly.

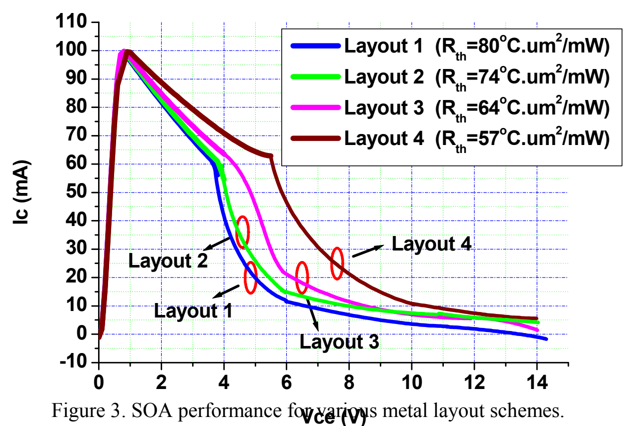


Figure 3. SOA performance for various metal layout schemes.

DEVICE PERFORMANCES

RUGGEDNESS

In Table 1, we compare the best ruggedness performance for all available technologies. The H02U-00 technology produces good power performance and its ruggedness performance is suitable for CDMA applications. The H02U-10 technology has better ruggedness performance with slight trade-off in power performance. However, with the newly introduced HBT3 technology, we are able to produce a device that is able to survive up to V_{CE}=5V at the P_{out}=37dBm under severe load mismatch condition (VSWR=12:1 or open load) for all phases, while the power performance is on par with the best available technology.

TABLE 1
Power and ruggedness performance comparison for different HBT technologies

Test condition: f=900MHz, VCE=3.6V, Quiescent Current=200mA, Pout=35dBm

Technology	Code	Breakdown (BV_{CEO})	Power performances			Ruggedness Performance	
			Pout (dBm) MAX	Linear Gain (dB)	Peak PAE (%)	C.W Mode	C.W Mode Stability under Load Mismatch
HBT2	H02U-00	15V	36	15.8	60	Failed at 3.6V,VSWR 3:1	NA
	H02U-10	20V	35.77	15.7	58	Pass 3.6V, VSWR 12:1 Failed at 5V, VSWR 3:1	Spurious observed at VSWR 6:1
HBT3	H02U-41	16V	35.38	15.28	60	Pass 5V VSWR 12:1	Below -70dBc

Figure 3 shows the 900MHz loadpull measurement result for a 5760μm^2 GSM HBT3 technology discreet power cell. When biased at V_{CE}=3.6V and I_c=100mA (fixed V_{BE}) under CW operation without harmonic tuning, the discreet power cell is able to deliver 34.5dBm output power with a peak power-added efficiency (PAE) of 63%. The power density is 0.49mW/μm^2 normalized to the total emitter area. By tuning the power cell for maximum efficiency, we are able to achieve up to 67% PAE.

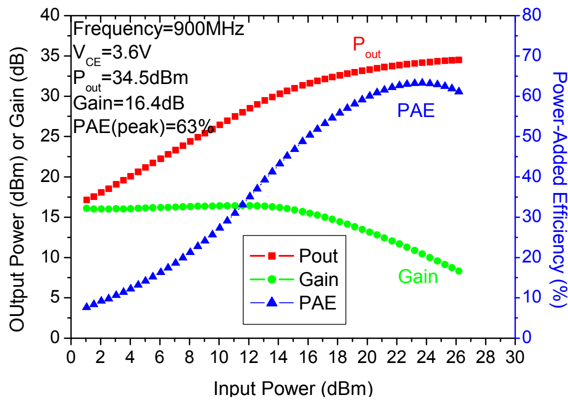


Figure 3. Loadpull measurement result for a 5760μm^2 GSM HBT3 technology discreet power cell at 900MHz.

The I-V curves at CW mode for a 11520μm^2 GSM HBT3 discreet power cell is shown in Figure 4. From the data, we can see that the device is able to operate up to a maximum current of 4.2A with 6W DC dissipated power on a FR4 evaluation board. Peak collector current density is able to reach 40kA/cm^2, indicating the device good current handling capability.

High ruggedness GSM MMIC PA products have been successfully designed by WIN's customers using our new HBT3 process. The PA designed using this technology is able to pass VSWR 15:1 with Vcc=4.7V under full power, demonstrating superior ruggedness performance.

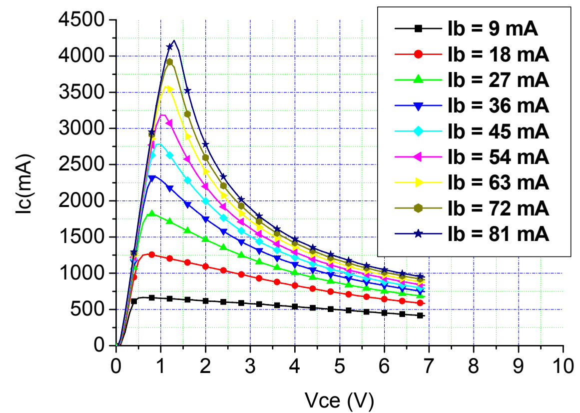


Figure 4. IV measurement for a 11520μm^2 GSM HBT3 technology discreet power cell.

LINEARITY

Figure 5 shows the SOA comparison for our CDMA HBT3 structure with our standard H02U-00 structure. As indicated, the on-state breakdown is significantly improved by over 3V depending on current density. This improvement provides the CDMA devices with a considerable margin to improve on its linearity performance.

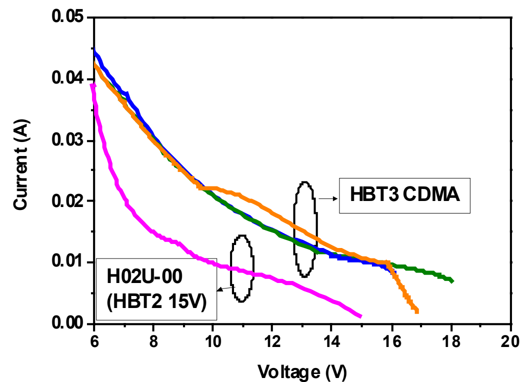


Figure 5. SOA comparison for CDMA HBT3 and H02U-00 15V technology (80μm^2 emitter device).

Table 2 compares the ACPR and PAE value for both technologies. We can note that the results are almost identical, indicating we are able to improve the ruggedness of the CDMA HBT3 structure without sacrificing any performance in linearity.

TABLE 2
ACPR comparison for 15V(H02U-00) and HBT3 technology.

H02U-00					
Pin [dBm]	**Pout [dBm]**	**Gain[dB]**	**PAE [%]**	**ACPR1Lo [dBc]**	**ACPR1Up [dBc]**
16.1	26.4	10.3	40.35	-40.6	-39.73
16.6	26.8	10.21	42	-38.36	-37.18
17.1	27.2	10.09	43.46	-35.89	-34.5
HBT3 technology					
Pin [dBm]	**Pout [dBm]**	**Gain [dB]**	**PAE [%]**	**ACPR1Lo [dBc]**	**ACPR1Up [dBc]**
16.25	25.71	9.46	33.22	-41.48	-43.57
17.25	26.75	9.5	37.21	-41.6	-42.74
18.32	27.74	9.42	41.2	-39.41	-38.41

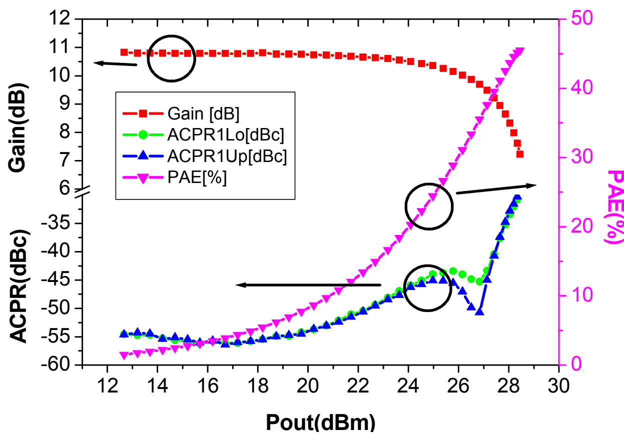


Figure 6. The measured power gain, PAE, ACPR1, and ACPR2 with W-CDMA modulation signal at 1.9GHz versus output power for a 5760μm^2 power cell fabricated with the HBT3 process.

Figure 6 shows the sweep ACPR and PAE results with WCDMA modulation signal at 1.9GHz for CDMA HBT3 device. At the output power of 27.5 dBm, the device achieves a PAE of 40% and ACPR better than -40 dBc simultaneously, using a simple capacitive matching network on FR4 evaluation board.

CONCLUSIONS

We report on our new generation HBT3 processes, showing noteworthy improvement in the device ruggedness performance, without compromising on all other major parameters. Valuable chip size reduction is achieved with improvement in metal scheme, cell layout and wafer processing techniques.

ACKNOWLEDGEMENTS

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REFERENCES

[1] T. Niwa, et. al., *A Composite-Collector InGaP/GaAs HBT with High Ruggedness for GSM Power Amplifier*,2003 IEEE MTT-S Digest, 2003.

ACRONYMS

HBT: Heterojunction Bipolar Transistor
GSM: Global System for Mobile Communications
CDMA: Code Division Multiple Access
WLAN: Wireless Local Area Network