A High-Performance 0.13-μm AlGaAs/InGaAs pHEMT Process Using Sidewall Spacer Technology

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ABSTRACT

A robust and manufacturable high-performance 0.13 μm gate length AlGaAs/InGaAs pseudomorphic High-Electron Mobility Transistor (pHEMT) process on 150 mm substrates is presented. This process, named TQP13, is unique in that the 0.13 μm gate lengths are achieved using cost effective I-line photolithography in conjunction with sidewall spacer technology. The process features a depletion-mode transistor with a nominal pinch-off voltage of –300 mV, on-resistance of 0.8 ohm-mm, extrinisic transconductance of 750 mS/mm, gate-to-drain breakdown voltage of 9 V, unity current gain cut-off frequency of 110 GHz (peak), maximum frequency of oscillation of >200 GHz, Idss of 90 mA/mm, and Imax (Vgs=+0.7 V) of 500 mA/mm. Passive components include 0.34 fF/μm^2 MIM capacitors, 105 ohm/square epitaxial resistors, precision 50 ohm/square NiCr resistors, and low-loss inductors using three levels of metallizations, two local and one airbridge. A wide variety of applications can be realized over a broad frequency range including low-noise amplifiers for consumer Direct Broadcast Satellite dish systems (Ku-band) and medium power amplifiers for automotive radar (W-band), for example.

INTRODUCTION

In this paper, we discuss a robust 0.13 μm gate length AlGaAs/InGaAs pHEMT process which is manufactured on TriQuint Oregon's 150 mm production line. This process is unique in that the 0.13 μm gate lengths are achieved using cost effective I-line photolithography resist and equipment in conjunction with sidewall spacers, a technique utilized in Silicon CMOS fabrication [1]. This key aspect differentiates the process from other sub-0.25 μm III-V FET-based technologies, which dedicate expensive tools such as deep-UV or e-beam systems to define the gate. The use of an I-line stepper, the workhorse of the semiconductor industry, enables a 0.13 μm process which provides a true high-volume, low-cost solution for high-performance circuits.

This process was incorporated into TriQuint Oregon's technology portfolio as part of the acquisition of Infineon's GaAs business. The technology transfer included adapting the process and epitaxy for the unit process capabilities and tool set present in Oregon's 150 mm production line [2]. The process, now called TQP13, has been successfully transferred and now matches and for some key parameters exceeds the performance of the original 0.13 μm HEMT110 process at Infineon.

A description of the 0.13 μm gate pHEMT process technology will be given as well as some typical dc, small-signal rf, and noise characteristics. Some circuit results are also presented to demonstrate the capabilities of the process.

PROCESS ARCHITECTURE

The epitaxial layers were deposited on GaAs substrates using Molecular Beam Epitaxy (MBE). The growth sequence begins with the formation of a superlattice buffer of alternating layers of GaAs and AlGaAs deposited on the substrate. AlGaAs spacer layers are placed on either side of the InGaAs channel with delta-doped layers placed on both sides of the channel-spacer layer stack. An AlGaAs Schottky layer is placed on top on the upper spacer layer in order to target the desired pinch-off voltage and transconductance. An N^+ GaAs ohmic contact layer is placed above the Schottky layer.

The TQP13 fabrication begins with the definition of alignment fiducials. A blanket film of plasma-enhanced chemical vapor dielectric is then deposited to passivate and protect the surface from subsequent process steps. After passivation, implant isolation is performed to define the active regions. Gate formation begins with the use of standard I-line lithography photoresist and equipment. The gate lengths are relatively large at this point but can be defined very uniformly and repeatably using the I-line stepper at this feature size. The final gate length of 0.13 μm is achieved through the application of a process used extensively in Silicon CMOS fabrication; sidewall spacers. Figures 1 (a) – (d) below illustrate the sidewall spacer concept as applied to TQP13. After the initial gate opening definition (see Fig. 1a), a thick layer of dielectric is deposited over the wafer (see Fig. 1b). This dielectric conformally covers and subsequently "fills in" the larger opening. The dielectric is then etched back using a plasma etch system which removes the dielectric over the field and within the opening (see Fig. 1c). Dielectric spacers remain along the sidewalls of the opening due to the anisotropy of the plasma etch (see Fig. 1d). These sidewall spacers produce a resultant feature size that is significantly smaller than the initial stepper-defined dimension.

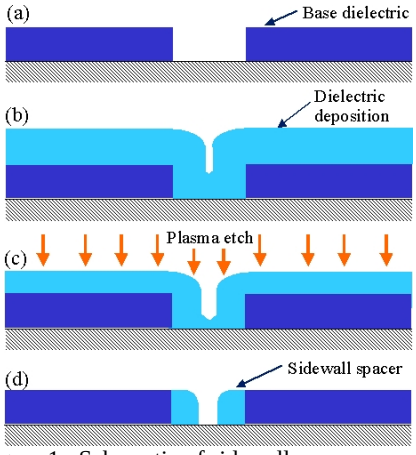

Figure 1: Schematic of sidewall spacer concept

Once the 0.13 µm gate opening is defined, a blanket film of refractory metal is sputtered over the wafer. Next, the Gate Reinforcement (GMET) layer consisting of Ti/Pt/Au metallization is aligned and patterned over the underlying gate feature. The Gate Reinforcement layer defines the upper portion of the gate contact. It is also used as a mask during the etch removal of the refractory metal from the field. After the blanket etch, the remained metal under the GMET defines the lower portion or "trunk" of the gate contact. The final gate contact is "T"-shaped and simultaneously allows for both ultra-short 0.13 µm gates and very low gate resistance. The sheet resistivity of the GMET metallization is 50 mohm/sq. The use of refractory metals also allows for a thermally stable contact, thereby avoiding gate sinking effects which can be present with the commonly used Ti/Pt/Au gate metallization.

Upon completion of the gate contact, the ohmic contacts are then defined. The GMET is used as a mask during deposition of the Au/Ge/Ni/Au metallization, thus allowing for the ohmics to be self-aligned to the gate contact. The close proximity of the ohmics to the gate contacts minimizes the resistive parasitics and thus facilitates high performance transistors. The on-resistance and drain/source resistances are <0.8 ohm-mm and <0.4 ohm-mm, respectively. Epitaxial resistors with sheet resistivity of 105 ohm/sq are formed using the ohmic metallization and un-isolated regions of the epitaxial layer. Figure 2 shows a schematic of the TQP13 transistor.

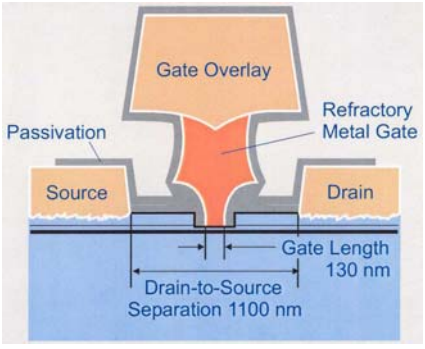

Figure 2: Schematic of TQP13 transistor.

The interconnects consist of the following layers: MIM-Bottom (MBOT), Bell Metal (BELL), and Airbridge. The MIM-Bottom layer is a 1 µm thick Ti/Pt/Au metallization and is used as the bottom plate of MIM capacitors. The Bell Metal layer is also a 1 µm thick Ti/Pt/Au metallization but is used as the top plate of MIM capacitors. These layers in conjunction with a 5 um thick electroplated Au Airbridge layer may be used to form high-Q inductors and for global wiring purposes. Sandwiched between the MBOT and BELL is a 190 nm thick layer of dielectric which serves as the MIM capacitor. The MIM capacitor has a relative permittivity of 6.8 and a capacitance per unit area of 0.34 fF/µm^2. Precision 50 ohm/square Nickel-Chromium (NiCr) resistors are also possible for this process. A representative schematic cross-section of the complete process architecture is shown in Fig. 3 below.

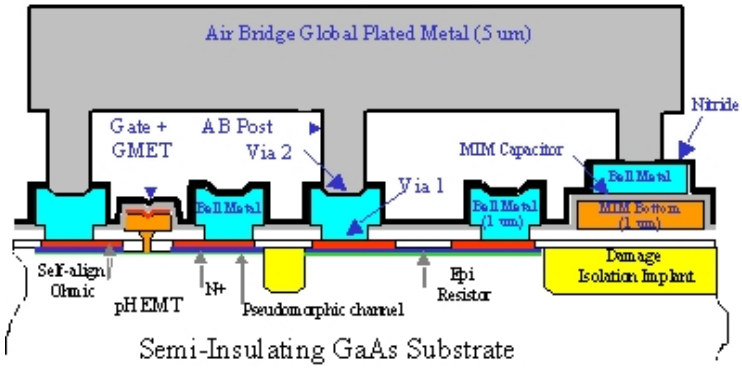

Figure 3: Schematic cross-section of the TQP13 process

Upon completion of front-side processing, the wafers can be finished in a variety of ways. The options include: thinning the substrate down to thicknesses of 100, 175, or 250 µm; sawing; and/or substrate via formation for front-side connection to a backside ground plane.

A detailed process qualification has been completed and included wafer level and packaged product testing. The wafer level reliability testing included autoclave at 121°C, 100% relative humidity, and 15 psi for 96 hours, high temperature unbiased bake at 275°C in air for 168 hours, and temperature cycle from –40 to +125°C for 1000 cycles. The packaged product reliability testing included HTOL under bias and at 150°C junction temperature. Life-test was also completed on transistors subjected to junction temperatures of 255, 270, and 285 °C. Based on the three temperature life-test, the activation energy was extrapolated to be >1.8 eV. For the junction temperature of 150°C, the mean time to failure (MTTF) for TQP13 transistors is >5E7 hrs.

DEVICE AND CIRCUIT PERFORMANCE

Figures 4 and 5 below show the current-voltage (Ids-Vds) and transfer characteristics, respectively, of a typical TQP13 transistor. As can be seen in the figures, the characteristics for these ultra-short gate length devices are well-behaved and exhibit no kink effects or spurious points/peaks. The devices also have good pinch-off

characteristics. The Imax (Vgs=+0.7 V) is 500 mA/mm at a Vds of 2.0 V and the peak extrinsic transconductance (Gm) exceeds 750 mS/mm. The gate-to-drain breakdown voltage, defined at a gate reverse current of 1 mA/mm, is typically 9 V.

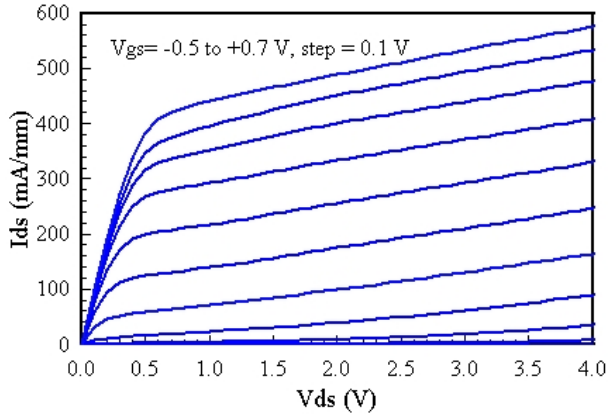

Figure 4: Ids vs. Vds relationship.

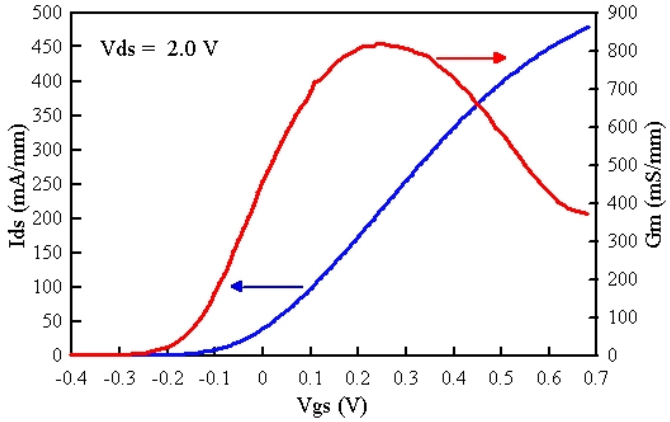

Figure 5: Transfer characteristics (Ids and Gm vs. Vgs).

Figure 6 below shows the unity current gain cut-off frequency (Ft) as a function of drain current at various drain-source voltages.

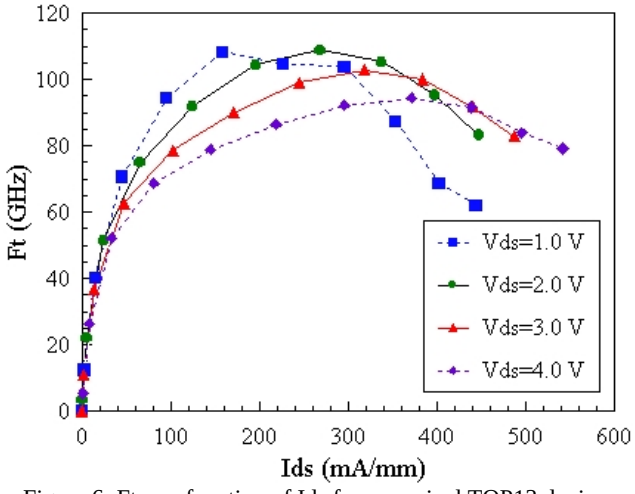

Figure 6: Ft as a function of Ids for a nominal TQP13 device.

Table 1 summarizes the nominal DC and RF parametrics for the TQP13 transistors and values for the passive elements.

Table 1: TQP13 Process Details

Typical Specifications		
Parameter	**Value**	**Units**
Vp	-0.3	V
Idss	90	mA/mm
Imax (Vg = +0.7)	500	mA/mm
Gm (max)	750	mS/mm
Bvdgo	9	V
Ron	0.8	ohm-mm
Ft (peak)	110	GHz
Fmax	>200	GHz
Process Elements		
Parameter	**Value**	**Units**
MIM Cap	0.34	fF/μm^2
Resistors	105	ohm/sq
MBOT (1 μm)	30	mohm/sq
Bell Metal (1 μm)	30	mohm/sq
Airbridge (5 μm)	4.5	mohm/sq

The noise performance of the TQP13 transistors was evaluated and is shown in Figure 7. The noise figure (Fmin) at a measurement frequency of 10 GHz was below 0.4 dB for drain currents under 150 mA/mm. At a measurement frequency of 18 GHz , the Fmin is approximately 0.7 dB for drain currents under 150 mA/mm. These results show that the process is highly suitable for LNAs in the Ku frequency band.

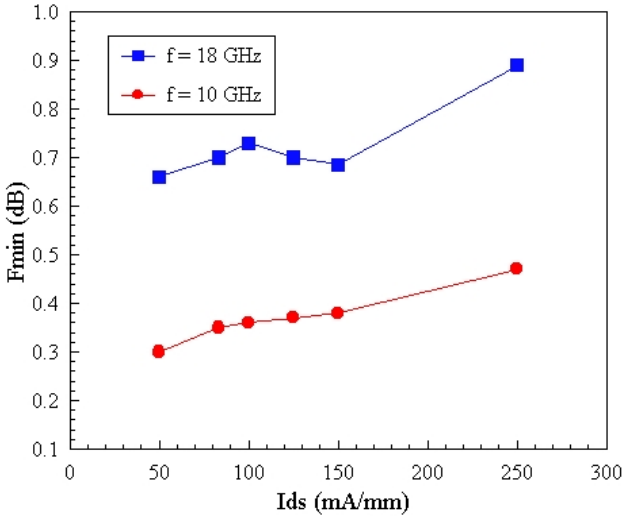

Figure 7: Noise figure as a function of drain current at frequencies of 10 and 18 GHz.

The TQP13 process is particularly attractive as a low-cost solution for the consumer market in Direct Broadcast Satellite (DBS) receiver systems. For example, one such

product is the CFH120. The CFH120 is unique in that it is a 12 GHz LNA, which is encapsulated within a simple, low-cost SOT-style plastic overmold package. Typically, packages of this type are avoided in products at this frequency due to the parasitics introduced by the overmold. These parasitics effectively degrade the gain of the transistor and thus more expensive open cavity packaging options are preferred. The TQP13 process, on the other hand, has ample gain at 12GHz, even when encapsulated within plastic overmold. The combination of a low-cost, high-performance process and low-cost packaging options allows for tremendous flexibility in designing solutions for DBS systems and other higher frequency applications. Table 2 below shows the electrical characteristics of the CFH120.

Table 2: CFH120 Specifications (in SOT-style package)

Electrical Characteristics (Vds = 2.0V, Ids = 10 mA, Freq = 12 GHz)	
Transconductance (mS)	60
Noise Figure (dB)	0.5
Associated Gain (dB)	13

While the TQP13 process is an ideal candidate for consumer DBS systems, the process is also suitable for the very high frequency W-band applications such as automotive radar. GaAs pHEMTs are the preferred technology for automotive radar components due their capabilities; including high output power and gain, low-noise figure, process maturity and reliability, and low cost. A critical component of automotive radar front-end systems is the 77 GHz transmitter. Figure 8 shows a chip photo of a 77 GHz two-stage medium power amplifier (MPA), which was designed and fabricated in TQP13. The chip size was 1.35 x 1.05 mm. Figure 9 shows the gain and output power vs. input power at a measurement frequency of 77 GHz. The MPA achieves 12.5 dBm of P-1dB output power and 16.5 dBm of saturated output power. These characteristics are state-of-the-art and demonstrate the capabilities of the process.

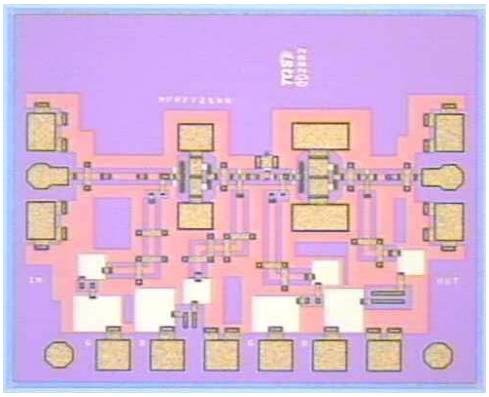

Figure 8: Photo of 77 GHz 2-stage Medium Power Amplifier.

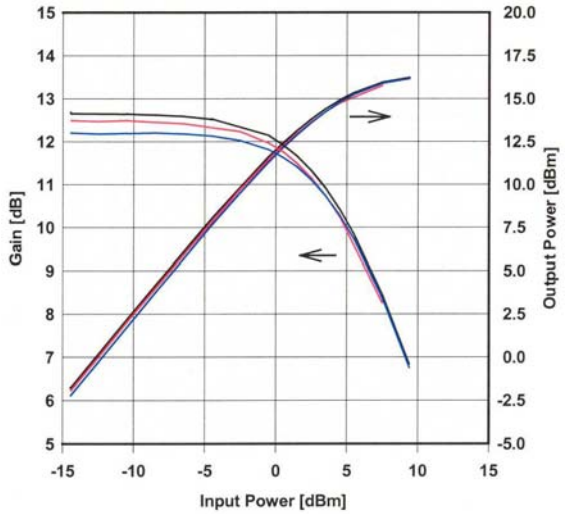

Figure 9: Gain and Pout of 77 GHz 2-Stage Medium Power Amplifier for automotive radar applications.

CONCLUSIONS

A detailed description of the TQP13 process architecture has been presented along with representative device and circuit performance. This robust and manufacturable process can be used for a wide variety of applications.

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[2] G. Mahoney et al. GaAs MANTECH Technical Digest, pp. 75-78. April 2004.

ACRONYMS

BELL: Bell Metal
DBS: Direct Broadcast Satellite
GMET: Gate Reinforcement layer
HTOL: High temperature operating life
LNA: Low-noise amplifiers
MBE: Molecular Beam Epitaxy
MBOT: MIM Bottom
MIM: Metal-Insulator-Metal
MTTF: Mean time to failure
MPA: Medium power amplifier
PHEMT: Pseudomorphic high-electron mobility transistor