# All i-line lift-off T-gate process and materials

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**Abstract**

**An all i-line 0.22 um T-gate process is demonstrated. A resist structure suitable for metal deposition and lift-off is constructed sequentially with two different resist materials. The lithographic process is described in details in this paper.**

## INTRODUCTION

The lift-off process is used widely for depositing metal layers where dry etching of metal is undesirable. Plasma etching of metal in such cases can cause damage to the device or other adverse effects. Therefore, the lift-off process is commonly used in GaAs and compound semiconductor wafer processing. T-gate construction employing the lift-off process requires multiple resist layers and frequently more than one exposure tool / regime processing. It is common practice to use e-beam to expose the first resist layer, followed by i-line exposure for the following layer process to produce sub 0.5 um gates. A single e-beam exposure process has been recently developed for sub 100nm T-gate construction, however, it requires a tri-layer resist stack [(1)]. Other than the resolution limitations, an all i-line process is more desirable because it can be more efficient and economic than e-beam / i-line multiple exposure tools process.

## RESIST PROCESSING AND MATERIALS

*Process outline*

The full process sequence is illustrated in the schematic drawing of Figure 1. The full process consists of five basic steps. The first three lithographic steps were experimentally demonstrated in this paper to construct a suitable lift-off resist structure for the gate metal deposition (step 4). The resist structure is easily removed in step 5 using appropriate stripper or organic solvents.

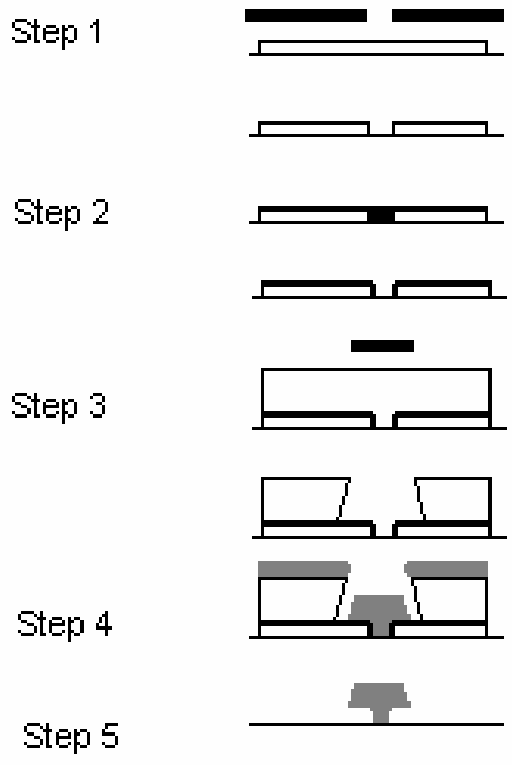


Figure 1:
The full T-gate lift-off process outline is represented in 5 steps. The first 3 steps employ two resist materials to construct a suitable lift-off structure for metal deposition and successful removal of all resist in steps 4 and 5.

The first resist is processed in step 1 to print isolated trenches directly over GaAs substrate. An intermediate barrier of thin organic coating is applied and processed over the resist trenches in step 2. The top resist layer is applied and processed in step 3.

All materials are produced and provided by AZ Electronic Materials.

*Process details*

*Step 1.*

First layer, AZ® HiR™-1075 positive resist:
Soft bakes: 90°C for 80 seconds.

Post exposure bakes (PEB): 115°C for 80 seconds, contact bake.
Exposure tool: 0.57NA ASML 5500/100D i-line stepper

Development: commercially available aqueous alkaline developer: AZ® MIF-300 for 70 seconds single puddle.

The thickness of the first resist layer, AZ® HiR™-1075 is 0.24 um, in which 0.375 um trenches are printed with i-line radiation.
AZ® 7908 resists has also been tried successfully in a similar process.

*Step 2*.
A layer of RELACS™ [2],[3],[4] is applied over the processed positive resist, baked, developed and reflowed thermally.

The RELACS material, AZ® R-500 Coating, is spin coated from an aqueous solution. Soft baked at 70°C for 70 seconds then diffusion baked at 135°C for 60 seconds and chilled at 21°C for 45 seconds. Only a thin layer of the RELACS™ coating, which is in direct contact with the resist surfaces, is thermally crosslinked during the diffusion baking step. The acidity of the resin present in the positive resist coating is believed to be sufficient to activate the RELACS™ crosslinking in contact with it. The excess, uncrosslinked RELACS™ material at the top of the resist and the trenches is developed out with DI water base developer for 55 seconds. A thin insoluble, conformable, layer of crosslinked RELACS™ remains only at the resist top and its sidewall surfaces. The RELACS™ material is completely washed out in the open trenches.

As a result of the RELACS™ process, the trenches size shrink to 0.22 um. The desired trench side wall slopes and top corner rounding, required for the gate process, is produced by the resist reflow during the diffusion bake. This process also removes any standing wave effects on the resist sidewalls.

The insoluble RELACS™ layer acts as a barrier layer to allow the application of the second top resist without interlayer mixing.

*Step 3*.
The second resist layer is 1.17 um thick, negative lift-off resist, AZ® EXP nLOF® 2173-145R2 applied on top of the processed trench structures.
Soft baked at 110°C for 80 seconds,
Exposure tool: 0.57NA ASML 5500/100D i-line stepper
PEB at 110°C for 80 seconds, contact bake
Development: AZ® MIF-300 developer, puddle mode.

The developed trenches are 0.8 um wide with inverted profiles. The second set of trench pattern is aligned over the first set to print the desired structure.

The resulting resist stack structure is shown over GaAs substrate in Figure 2.

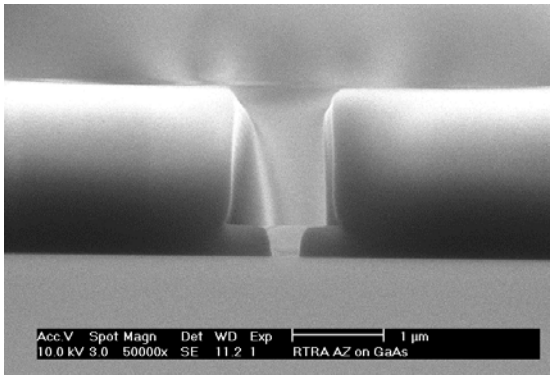


Figure 2:
Two layer resist stack structure suitable for the construction of T-gate on GaAs substrate, via metal deposition /lift-off process. This structure is all i-line processed with a lower positive resist and a top negative lift-off resist

Courtesy of Richard Travers, ASML Special Applications

## CONCLUSIONS

The total resist stack structure, shown in Figure 2, is suitable to construct the final metal gate structure. The metal deposition is directed to the center of the trenches, by the shadowing effect of the inverted top resist profiles. Thus, the bottom trenches can be completely filled with deposited metal and form the T gates, without touching the upper resist sidewalls.

The inverted negative resist side wall profiles prevent the metal from filling the upper trenches and allow the lift-off process to completely strip the resist stack.

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