A Novel Process for Reduced Dispersion Effects in AlGaN/GaN HEMTs

James Gillespie, Antonio Crespo, Robert Fitch, Gregg Jessen, Derrick Langley,
Neil Moser, Dave Via, Matthew Williams, Mark Yannazzi

Air Force Research Laboratory
2241 Avionics Circle, Wright-Patterson AFB, Ohio

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Abstract – **Effects of early deposition of Si_3N_4 passivation on AlGaN/GaN HEMTs have been studied as it relates to RF dispersion, breakdown voltage and X-band power. Two AlGaN/GaN epitaxial wafers grown on SiC substrates together in one lot were used. These wafers were processed using a common process with one exception. One wafer had Si_3N_4 deposited before processing began while the other one was processed using a standard passivation process after gate deposition. The results show improved rf dispersion characteristics (< 5% I_{dss} reduction), higher breakdown voltages (40volts) and superior power results (> 8.4W/mm @ 33% PAE) for the wafer which had early deposition of Si_3N_4 passivation.**

I. Introduction

Military and commercial requirements for high power and high frequency amplifiers have driven the development of AlGaN/GaN High Electron Mobility transistors. (HEMTs) However, this material technology has demonstrated large discrepancies in projected RF power measurements based on DC-IV measurements and actual RF power measurements. By using high-speed pulsed DC measurements I_{max} has been shown to collapse by as much as 70%. [1] Surface traps between the gate and the drain are thought to cause the device to effectively pinch-off during high-speed operation. [2] These traps can fill with electrons at device bias conditions and reduce sheet charge between the gate and drain of the device. Passivating the device with silicon nitride has been shown to reduce the trapping affects and dispersion but not completely eliminate it. It has been reported that post-deposition annealing of silicon nitride (Si_3N_4) improves its electrical properties as a gate dielectric in some devices. [3] This work focuses on improving the silicon nitride-to-AlGaN interface for better pinning of the surface states by using a passivation first process, which includes a post-deposition anneal.

II. Experiment

Material used in this experiment was grown on SiC wafers using Metal Organic Chemical Vapor Deposition (MOCVD). Both wafers were grown together. Mobility and Sheet charge were 1000-1200 $cm^2\ V^{-1}$ sec and $1x10^{13}cm^{-2}$, respectively. In order to make direct comparisons, both wafers were processed together when possible. One wafer had Si_3N_4 deposition performed as the first step. Then both wafers went through a mesa etch step. This was performed using a chlorine based Inductively Coupled Plasma (ICP) etch tool to etch 500Å into the GaN buffer. For the Si_3N_4 1st sample the Si_3N_4 was first removed using Freon 14 Reactive Ion Etch (RIE) process. Both wafers went through ohmic lithography together. The Si_3N_4 1st sample had the Si_3N_4 removed just prior to ohmic metalization. A gate footprint window was etched in the Si_3N_4 prior to ohmic alloy. Both wafers were alloyed using a nitrogen environment rapid thermal process of 850ºC for 30 seconds. After ohmic alloy the wafers were processed together for optical gates. Figure 1 shows a

gate cross-section of the Si_3N_4 1st process. The gate footprint for this process is 0.8μm

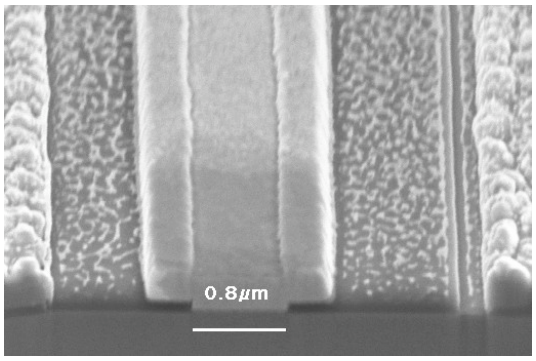

Figure 1. Silicon Nitride 1st processed gate cross-section

III. Measurements and Results

Devices on both wafers were measured for DC and RF parameters using cascade probes with an HP8510C Vector Network Analyzer and an HP4142 parameter analyzer. Pulsed DC IV measurements were made using an Accent Dynamic IV Analyzer. (DIVA) All pulse measurements used 0.2 µs wide pulses separated by 2 ms. Power measurements were made using an on wafer Murray load pull system. Sheet and contact resistances were obtained from the Transfer Length Method (TLM) measured using a Keithley 450 Parametric Analyzer. Sheet resistance for both wafers was 355 Ω/sq. Contact resistance increased for the Si_3N_4 first processed wafer from 0.43 Ω-mm to 0.633 Ω-mm. Three terminal breakdown voltage was measured to be 80 volts for both wafers at 1mA/mm at V_g = -6v. Figure 2 shows a decrease in dispersion as well as an increase in I_{dss} for the Si_3N_4 1st sample. Gate leakage was reduced by a factor of 2 for the devices processed using the Si_3N_4 1st process and is shown in Figure 3. F_t values were 15GHz for the silicon nitride first process and 10GHz for the standard processed wafer. F_{max} values were 25GHz and 35GHz respectively. Power results showed a dramatic improvement between the standard process and the experimental process. Figure 4 shows the results of load pull measurements for this process. This result was 8.4W/mm compared to the standard processed wafer of 2.4W/mm. All power measurements were taken at 8.5GHz.

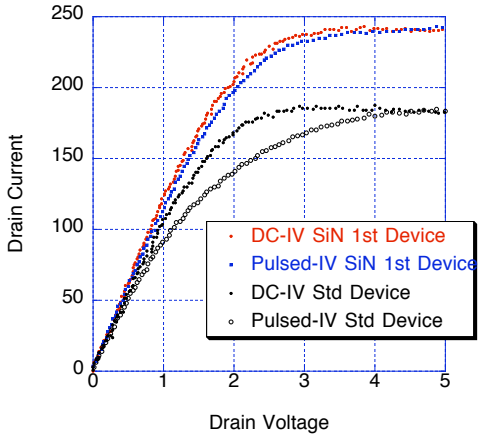

Figure 2. DC vs pulsed IV for Si3N4 1st and standard processed devices. Pulsed bias conditions Vds = 20v, Vgs = -7v

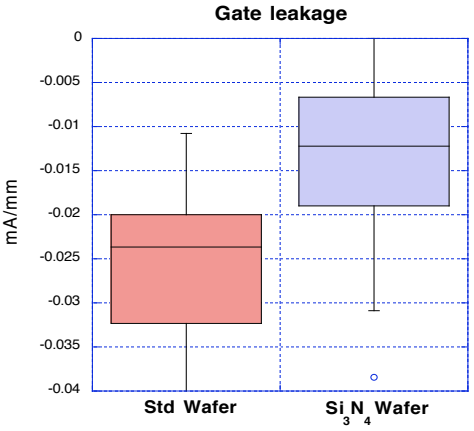

Figure 3. Boxplots of gate leakage measured on standard and experimental processed wafer

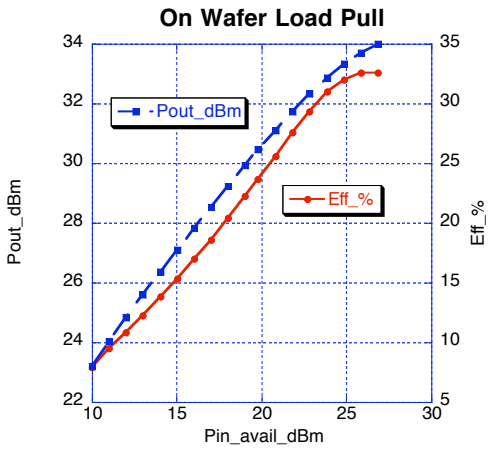

Figure 4. Pout and efficiency as a function of available input power for silicon nitride 1st process.

The improved F_t values were a result of a smaller gate length for the improved Si_3N_4 1st process. This is a result of being able to define a smaller gate footprint in the Si_3N_4 film. The reduction in F_{max} was due to the overlap of the gate on the Si_3N_4. This effectively created a field plate device and increases C_{gs} which reduces F_{max}. When electron beam defined devices are processed using this technique a better comparison will be made as to the effects of frequency improvement.

IV. Conclusion

We presented results from a novel AlGaN/GaN HEMT process. This process made use of depositing Si_3N_4 on the surface of the AlGaN prior to device processing. This allowed the AlGaN surface and Si_3N_4 to go through the ohmic alloy process together. This 850ºC process is assumed to have created a better interface and reduced RF dispersion. The gate footprint was defined in the Si_3N_4 film prior to ohmic alloy. The alloy was believed to reduce the etch damage prior to schottky metal deposition. The resulting devices were shown to have, in addition to improved dispersion, increased drain current, reduced gate leakage and over 3.5 times improved power measurements.

V. Acknowledgements

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