Method for Determining Substrate Via Yield

Michael Meeder, Michael Fresina, Charles Whitman
RF Micro Devices, Inc. 7628 Thorndike Road, Greensboro, NC 27409
mmeeder@rfmd.com, 336-678-8295

Abstract

The substrate via (backside via) is an integral part of any GaAs power amplifier process and via yield is critical to performance. Further, the continuing need to decrease die size makes any reduction in substrate via diameter desirable. In this paper we propose a substrate via test structure that can be used along with simple statistical methods to determine the substrate via yield when making a process change or improvement. It can also be used to quantitatively compare different processes.

Introduction

For RF and microwave circuits, ground connections should have low loss and inductance in order to for the circuit to have good noise figure, VSWR, gain, power-added efficiency (PAE), and bandwidth [1]. In many GaAs MMIC processes, this function is served by substrate vias. A substrate via is an opening in the GaAs substrate made by wet or dry etching. The via holes are then metallized for electrical and thermal connection from the front of the die to the back.

As GaAs die continue to become smaller, the need for smaller substrate vias grows [2]. However, it must first be determined if a smaller diameter substrate via will have sufficient yield. An automated electrical test can effectively answer this question.

Experiment

The test structures were formed by connecting 100 vias using front side metal and patterned backside metal. The structures were designed to be probed using the Kelvin method for maximum accuracy [3]. The structures could be probed from the front or backside of the wafer. Test structures are given in Figures 1 and 2.

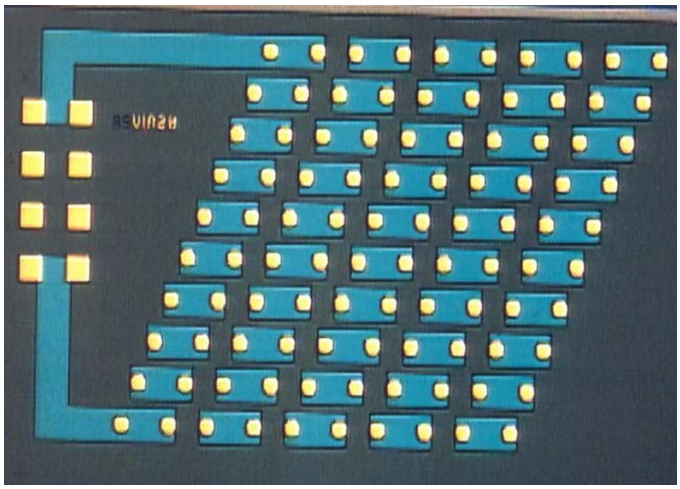

Figure 1: Front side of via chain

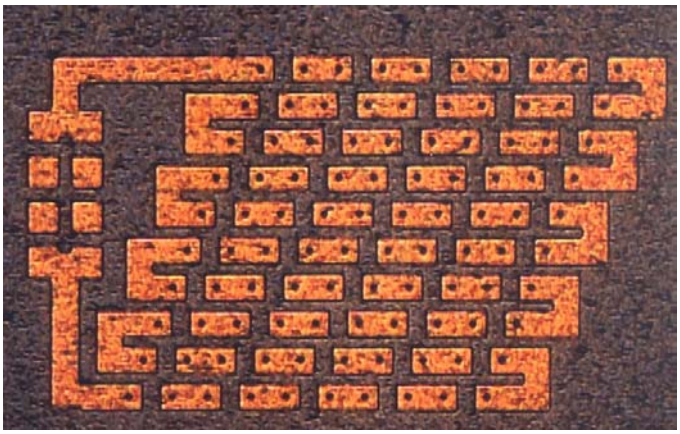

Figure 2: Back side of via chain

Multiple versions of the substrate via test structure were designed with varying via sizes. The metal interconnections between via holes were kept constant allowing differences in resistances between the these structures to be attributed to the via hole diameter.

As a thinned wafer could easily break during handling or testing, finished wafers were mounted to a silicon substrate. The wafers could be mounted front side up or backside up for testing. All structures were tested using an autoprober and measurements performed with a HP 4062 semiconductor parameter analyzer system.

A 150 mm wafer tested had 194 via chains where each via had a diameter of 50 um. With 100 vias per chain, a total of 19400 individual vias were tested. A histogram of the observed resistance values was used to define good and bad test structures.

Analysis

Figure 3 below shows the histogram of resistance values from a sample wafer. A via chain was considered bad if it had a resistance value larger than the mean + 3σ. The values shown in Figure 3 are those within ±3σ of the mean.

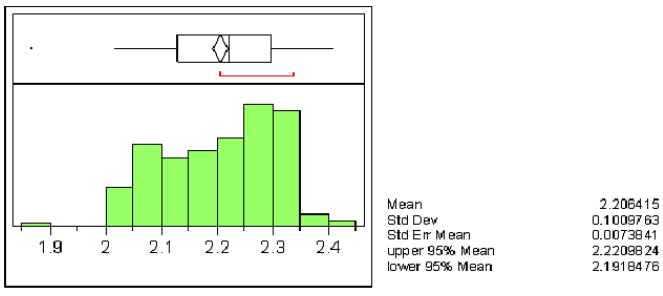

Figure 3: Histogram of resistance values

A simple reliability approach was used to predict the probability of failure for an individual via. Consider a chain of n independent vias shown symbolically in Figure 4.

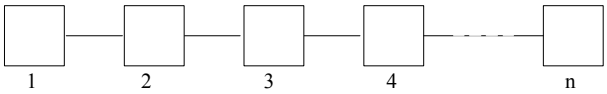

Figure 4: Symbolic representation of via chain

The reliability, of a chain of *n* independent vias in series (R_{chain}) where the entire chain fails if any individual via fails is given by [4]:

(1) $$R_{chain} = [R_{via}]^n$$

where R_{via} is the reliability of an individual via. Since $R = 1 - P$ where P is the probability of failure, we have

(2) $$1 - P_{chain} = (1 - P_{via})^n$$

Solving for P_{via} we obtain

(3) $$P_{via} = 1 - (1 - P_{chain})^{1/n}$$

P_{chain} is the fraction of chains that fail on a wafer. For a test wafer, suppose P_{chain} was 97/194 or 0.50 (50%). Inserting this value for P_{chain} into equation 3 with $n = 98$ results in a P_{via} of 0.007 or 0.7%. The standard error and a confidence interval for P_{via} can be determined using the binomial distribution. Statistical comparisons can be conducted across groups using the standard error, allowing quantitative comparisons. Processing wafers with the Kelvin structures along with wafers with product die on them would enable the characterization of wafers of importance (product wafers).

CONCLUSIONS

A variation in a standard via test structure has been developed for the GaAs substrate via. The substrate via test structure allows for a quantitative analysis of the substrate via yield of an individual wafer. Using the test structure along with a simple statistical method allows for quantitative comparison of multiple backside processes involving substrate vias. Future work will explore via chains of different lengths to test the independence assumption.

REFERENCES

[1] I. Bahl. Lumped Elements for RF and Microwave Circuits. 1st Ed, p. 279. 2003
[2] H.Hendriks, A.Hanson, T. Lepkowski, A. Quaglietta, and B. Patel. "Benefits and Challenges in Decreasing GaAs Through Substrate Via Size and Die Thickness." 2002 GaAs Mantech, p. 105.
[3] D.K. Schroder. Semiconductor Material and Device Characterization. 2nd Ed, p. 3. 1998.
[4] Tobias and Trindade, Applied Reliability. 2nd Ed, p. 31. 1995.

ACRONYMS

VSWR: Voltage Standing Wave Ratio
PAE: Power Added Efficiency
MMIC: Monolithic Microwave Integrated Circuit