InSb-based Quantum Well Transistors for High Speed, Low Power Applications

T. Ashley*, A. R. Barnes*, L. Buckle*, S. Datta†, A. B. Dean*, M. T. Emeny*, M. Fearn*, D. G. Hayes*, K. P. Hilton*, R. Jefferies*, T. Martin*, K. J. Nash*, T. J. Phillips*, W. H. A. Tang* and R. Chau†

*QinetiQ, Malvern Technology Center, St. Andrews Road, Malvern, WR14 3PS, UK
†Intel Corporation, Components Research, Logic Technology Development, Hillsboro, OR 97124, USA
Email: tjphillips@qinetiq.com

Abstract

InSb-based quantum well field-effect transistors with gate length down to 0.1 µm are fabricated for the first time. Room temperature electron mobilities of over 30,000 $cm^2V^{-1}s^{-1}$ are achieved with sheet carrier density greater than 1×10^{12} cm^{-2}. 0.1 µm gate length devices exhibit DC transconductance of 775 mS/mm with good output conductance and breakdown characteristics. RF measurements show an f_T of 210 GHz at V_{DS} = 0.5 V. Benchmarking against the state-of-the-art Si MOSFETs indicates that InSb QW transistors can achieve equivalent high speed performance with 5-10 times lower DC power dissipation, and, thus, can be a promising device technology to complement scaled silicon based devices for very low power, ultra-high speed logic applications.

1. Introduction

Indium antimonide (InSb) shows great promise as an ultra-fast, very low power technology as it has the highest electron mobility and saturation velocity of any known semiconductor (Table 1). This was earlier demonstrated in a carrier-extracted enhancement mode MISFET device, using an InSb device layer on an InSb substrate with a deposited SiO_2 gate oxide [1]. In this paper, we report the materials growth, device fabrication and characterisation of an InSb channel quantum well FET, which uses a semi-insulating GaAs substrate, a relaxed metamorphic buffer layer of $Al_yIn_{1-y}Sb$, a compressively strained InSb quantum well confined between layers of $Al_xIn_{1-x}Sb$ and a Schottky barrier metal gate.

Table 1. Channel Electron Properties at 295K

	Si	GaAs	$In_{.53}Ga_{.47}As$	InAs	InSb
Electron Mobility ($cm^2V^{-1}s^{-1}$ $n_s=1X10^{12}/cm^2$)	600	4,600	7,800	16,000	30,000
Electron Saturation Velocity (10^7 cm/s)	1.0	1.2	0.8	3.5	5.0
Energy Band-gap	1.12	1.42	0.72	0.36	0.18

2. Materials Growth and Results

The InSb quantum well material is grown by molecular beam epitaxy (MBE) on a semi-insulating GaAs substrate. The layers from bottom to top consist of an accommodation layer, 3 µm $Al_yIn_{1-y}Sb$ buffer, optional $Al_xIn_{1-x}Sb$ bottom barrier, a 20 nm thick InSb quantum well, a 5 nm thick $Al_xIn_{1-x}Sb$ spacer, a Te δ-doped donor sheet (~1×10^{12} cm^{-2}) and, finally, a 15-45 nm thick $Al_xIn_{1-x}Sb$ top barrier layer. Single field Hall mobility measurements versus sheet carrier densities (n_s) are shown in Figure 1. The results show that, for a given carrier density, the quantum well mobility increases monotonically with increasing Al percentage from 15% to 30%. Hall mobility measurements show that with 30% Al in the barrier layers the quantum well mobility achieved is 30,000 $cm^2V^{-1}s^{-1}$ at n_s = 1.3×10^{12} cm^{-2}, which is above the bulk InSb mobility versus doping concentration trend-line.

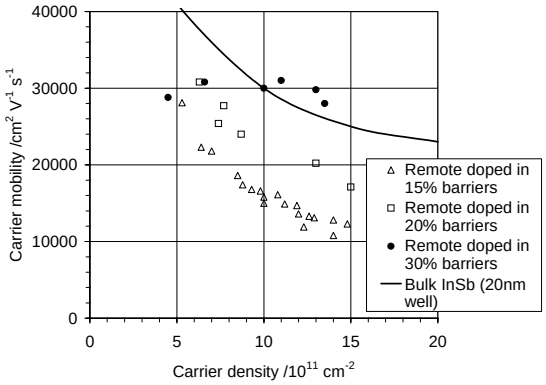

Figure 1. Hall mobility data on Te modulation doped 20 nm thick InSb quantum wells with 15%, 20% and 30% Al in the $Al_xIn_{1-x}Sb$ barrier layer, with the bulk doped equivalent shown for comparison.

3. Transistor Fabrication

The InSb quantum well transistors were fabricated with gate lengths in the range of 0.1-0.4 µm. The material used in the reported devices consists of a 20 nm modulation doped InSb quantum well between 20% Al barrier layers, with an average mobility of 25,000 $cm^2V^{-1}s^{-1}$ at n_s = 1.0×10^{12} cm^{-2}. First, in the fabrication process sequence, the source and drain ohmic contacts are defined using optical lithography, e-beam evaporation of Ti/Au and lift-off. The Ti/Au Schottky gate metallization is then performed using e-beam lithography and lift-off. Finally, device isolation is achieved by wet chemical etching which results in an air-bridge at the mesa edge between the channel and the gate and drain feed metal (Figure 2).

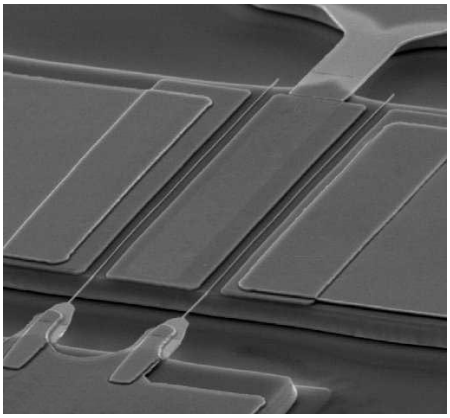

Figure 2. SEM micrograph of a two-finger InSb quantum well transistor with gate air-bridge at mesa edge. L_G = 0.1 µm, L_{DS} = 1.0 µm.

4. DC Characterisation

The typical room temperature output characteristics of a 0.1 µm transistor are shown in Figure 3. The device exhibits good saturation characteristics with a knee voltage of 0.2 V and an off-state breakdown voltage of over 1.2 V. The low field source-drain resistance of this device is 1.1 Ω mm, with source-drain separation of 1 µm and an ohmic contact resistance of 0.25 Ω mm.

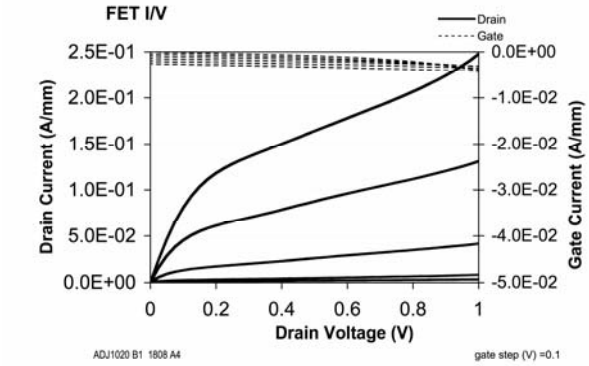

Figure 3. 0.1 µm L_G InSb QW transistor output characteristics at 295 K, L_{DS} = 1 µm, W_G = 40 µm, V_{GS} = 0.1 V/step.

Figure 4 shows the transfer characteristics of the device at V_{DS} = 0.5 V and 50 mV. The peak g_m for this device is 800 mS mm^{-1} at V_{DS} = 0.5 V. The device shows an on-current of 250 mA mm^{-1}, off-current of 2.0 mA mm^{-1}, and a sub-threshold slope of 120 mV/decade at V_{DS} = 0.5 V. The off-state current is limited by gate to drain leakage as shown in Figure 4, which may be reduced by optimising the Schottky contact.

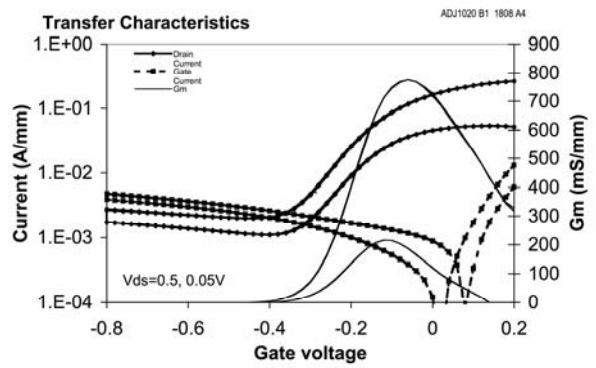

Figure 4. 0.1 µm L_G InSb QW transistor transfer characteristics at 295 K, L_{DS} = 1 µm, W_G = 40 µm, V_{DS} = 0.5 V and 0.05 V.

5. High Frequency Characterisation

RF characteristics of the InSb transistors were obtained at room temperature through on-wafer S-parameter measurements at frequencies up to 50 GHz. The parasitic capacitances associated with the probe pads were subtracted from the measured S-parameters through a Koolen de-embedding process. An f_T of 210 GHz was obtained by extrapolating $|h_{21}|^2$ with a slope of –20 dB/decade using a least squares fit. The maximum oscillation frequency f_{max} is around 270 GHz, yielding an f_{max}/f_T ratio of 1.3. Comparison of the f_T and DC power dissipation performance of state-of-the-art 80 nm gate Si nMOSFETs [2] with the InSb based quantum well FETs shows that the InSb transistors provide equivalent f_T at nearly 10 times lower power dissipation per unit width compared with the Si devices. The gate delay (CV/I) of InSb is also a factor of three lower than state-of-the-art and research Si transistors for equivalent gate length.

6. Conclusion

We have demonstrated for the first time InSb quantum well transistors with 0.1 µm gate length with comparable high frequency performance as state-of-the-art Si MOSFETs but with nearly 10 times lower DC power dissipation. This makes the InSb-based device technology a viable option for future generation ultra-high speed, very low power digital and RF applications. In future the challenge is to scale the gate length of InSb transistors aggressively to compete with extremely scaled CMOS transistors [3] while maintaining its performance-power advantage over Si.

References

[1] T. Ashley, A. B. Dean, C. T. Elliott, R. Jefferies, F. Khaleque and T. J. Phillips, IEDM Technical Digest, p.751 (1997).

[2] K. Kuhn, R. Basco, D. Becher, M. Hattendorf, P. Packan, I. Post, P. Vandervoorn and I. Young, Symposium on VLSI Technology (2004).

[3] R. Chau, B. Doyle, M. Doczy, S. Datta, S. Hareland, B. Jin, J. Kavalieros and M. Metz, Device Research Conference, p.123 (2003).