Student Paper

Edge Defined Lithography for Nano-scale III-N Field Effect Transistors

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Abstract

In this work we demonstrate a method by which sub-100 nm features can be fabricated using only conventional semiconductor processing and optical lithography techniques. This methodology uses no e-beam in the process but has the potential to create lithographically located features at dimensions approaching 5 nm. The successful process becomes an exercise in thin film process control, rather than lithography process control. To achieve this, we present several of the key issues surrounding the optimization process required to implement this technology and to exploit fully its potential.
Keywords: *Spacer Gate, Edge defined Lithography, MOSFET, GaN*

Introduction

Gate length scaling becomes cost prohibitive and difficult with e-beam technology alone for low volume production common in many compound semiconductor processes. While e-beam and other increasingly complicated lithography techniques have been successful to this end, we present another fabrication method that relies on a hybridization of conventional optical lithography and traditional semiconductor processing techniques. The introduction of a thin oxide in the process introduces the possibility of electrostatic discharge (ESD), thereby necessitating a non-ionizing approach to achieve minimum feature size. This method, commonly referred to as spacer gate fabrication[1-6], is able to generate features as small as 10 nm using only optical lithography and standard semiconductor processing tools. The principle tradeoff and drawback to this approach is that this method requires highly controlled thin film deposition and etch processes. To achieve these ends, a sequence of optimization procedures is required in order to exploit the technique's full potential. While the lift-off technique is dominate for GaAs and InP based devices, this work explores the possibility of a positive lithography technique designed specifically for sub-100 nm gate manufacturing in III-N based devices. This technique is more plausible and more suitable for the III-N system because of the increased resistance to chemical etches present in this material system.

The need for this arises from a recently identified oxide/GaN interface that demonstrates the capacity to control charge in excess of levels of $4 \cdot 10^{13}cm^{-2}$. The projected limit of this charge is expected to exceed $6 \cdot 10^{13}cm^{-2}$ in enhancement mode [3-5]. A comparable AlGaN/GaN based device is currently limited to $1.2 \cdot 10^{13}cm^{-2}$ [7]. The goal for the final device is shown in figure 1 and compared with the structure for a conventional GaN HFET. This approach is expected to address the demands of emerging mm-wave components for high power where low impedance approaches are more critical. The maximum current densities are expected to be 2 6 times as great for the MOS approach.

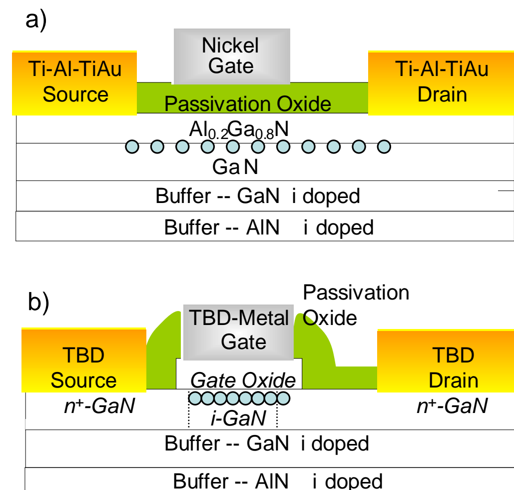

Figure 1: Conventional HFET architecture is shown above in figure (a). The intended use of the spacer gate process is for use in sub-100 nm gate length devices where e-beam lithography would not be practical. In a MOS configuration (b), charging effects limit the ability to use the e-beam lithography tool due to ESD effects.

Process Flow

A process flow for forming spacer gate structures in silicon based devices is shown in fig. 2. This method is readily adapted to the GaN MOSFET process. The first step in this original spacer gate fabrication process involves the deposition of a thin layer of a gate oxide on top of a silicon substrate. This is followed immediately by the subsequent deposition of two thin polysilicon layers and an SiO_2 layer. These depositions are carried out via a plasma enhanced chemical vapor deposition (PECVD). The top polysilicon layer is then patterned using conventional optical lithography techniques. Following the patterning of the sacrificial polysilicon layer, a thin layer of Si_3N_4 is deposited conformally over the entire wafer. These steps are summarized in fig. 2(a). This Si_3N_4 layer is then etched away using a highly anisotropic RIE process. Because of the conformality of the Si_3N_4 deposition and the anisotropy of the etch, what now remains

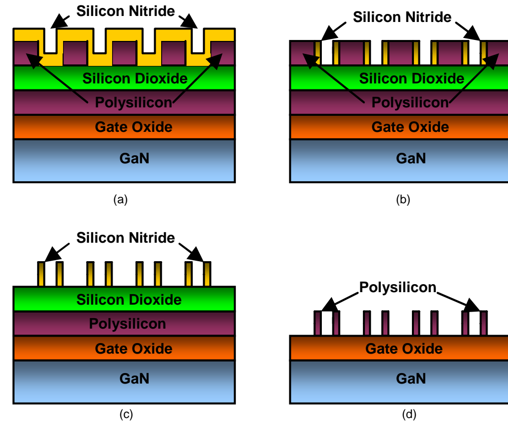

Figure 2: Spacer channel/gate structure fabrication cross-section. (a) Spacer channel/gate after deposition and patterning of the layers. (b) Spacer channel/gate after Si3N4 RIE. (c) Spacer channel/gate after polysilicon wet etch in KOH. (d) Spacer channel/gate after removal of remaining masking layers.

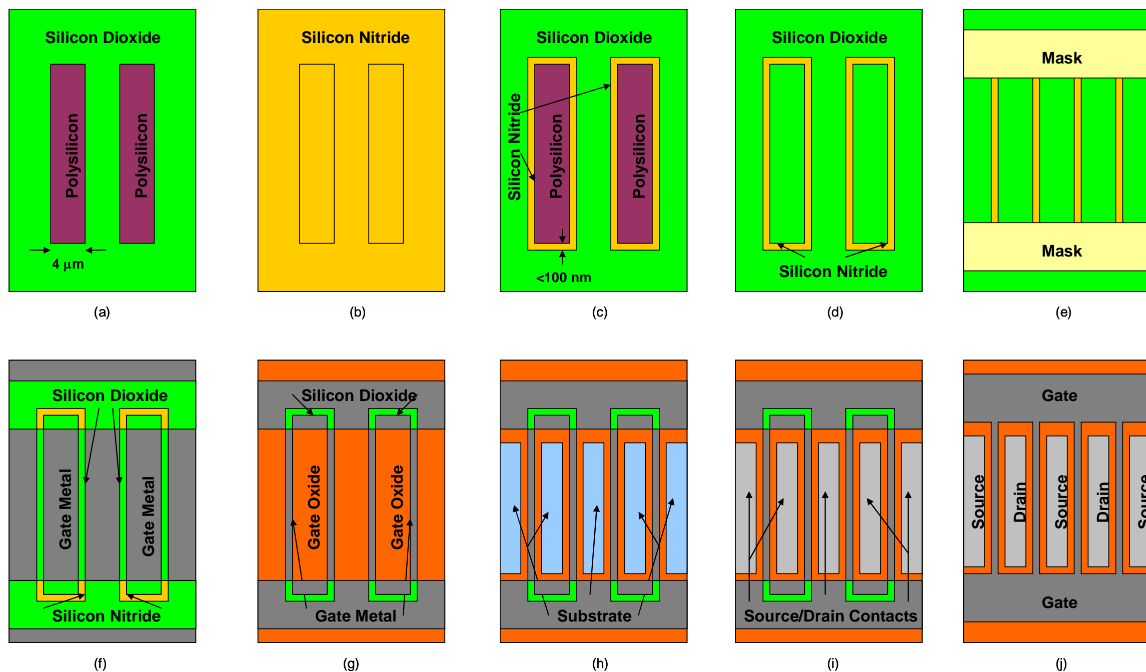

Figure 3: Top-down view of the proposed III-N transistor device fabrication process. (a) Photolithographically defined polysilicon mesas are formed. (b) Conformal deposition of Si_3N_4 over the entire surface. (c) RIE removal of the Si_3N_4 material. Only the thin side walls are left. (d) KOH is used to remove the polysilicon mesa, leaving the Si_3N_4 side walls intact. (e) A portion of the material is masked with photoresist to protect it from subsequent RIE processes. (f) An unselective RIE etch transfers the exposed pattern to the underlying layers, and the masking material is removed. (g) Another unselective RIE etch transfers the pattern down one additional layer. (h) Photolithography is used to define the source and drain regions, and that gate oxide is removed to expose the III-N substrate. (i) Source and drain contacts are formed over the exposed substrate. (j) BOE is used to remove any remaining SiO_2, leaving only the final device structure.

surrounding the polysilicon mesas are the very thin Si_3N_4 side walls, as shown in fig. 2(b). Following the RIE process, the polysilicon mesas are removed using a wet KOH etch. This leaves only the Si_3N_4 side walls, as shown in fig. 2(c). These structures serve as masks during subsequent etching. RIE processes are used to etch away the exposed portions of the SiO_2 layer, as well as the polysilicon layer underneath it. Following a brief HF "clean-up" etch to strip off any remaining masking layers, all that remains are the tiny polysilicon fins formed by the masking layers during the RIE etches. The final result is depicted in fig. 2(d). For the GaN approach, the poly-silicon can be used as a mask for a metal gate or the poly-silicon can be replaced by the required metal oxide gate stack.

These top down view and masks associated with each step is summarized in figure 3. Standard photolithography and RIE etching processes are used to create 4 µm wide mesas in the top polysilicon layer. A thin layer of Si_3N_4 is then deposited conformally over the surface of the wafer, which is followed immediately by the removal of this layer via an anisotropic RIE etch. The remaining Si_3N_4 side walls are less than 100 nm wide, as shown in fig. 3(c). A wet KOH etch is used to selectively remove the polysilicon mesas and to leave only the Si_3N_4 fins. Next, photoresist is used to mask off the top and bottom portions of the structure, and a nonselective RIE etch is performed. The portions of the structures underneath the photoresist remain unchanged, but the pattern of the exposed areas is transferred down one layer. After lifting off the photoresist mask, the structure appears as in fig. 3(f). Another nonselective RIE etch is performed in order to transfer the patterns down one last layer in the device structure, as seen in fig. 3(g). Once again, standard optical lithography and etching techniques are used in order to expose several areas of the III-N substrate. Source and drain contact metals are then deposited into these regions, as shown in figs. 3(h,i). Finally, a BOE etch is done in order to remove any residual SiO_2 from the structures. All that remains is the MOSFET device shown in fig. 3(j), which can in principle have a gate length as small as 10nm.

Initial attempts at forming such spacer gate structures resulted in features measuring approximately 200 ± 25 nm. SEM and AFM images of these early spacer gate structures are shown in figure 4. The targeted dimension for the structures, however, was 50nm. This structure was obtained with contact lithography alone and did not have the benefit of stepper based lithography. Post mortem analysis indicated that this discrepancy was due to the cumulative impact of poor process controls present in each of the individual fabrication steps. A huge range of spacer lengths was obtained, from not being present at all to having sizes that approach 0.5µm. To rectify the problem, process control was performed at in each step to bring the cumulative process in control

Process Optimization

The first step in such a solution involves simply depositing and etching thin films uniformly and at the appropriate rates. While there are undoubtedly other considerations in the overall process, given the delicate nature of the

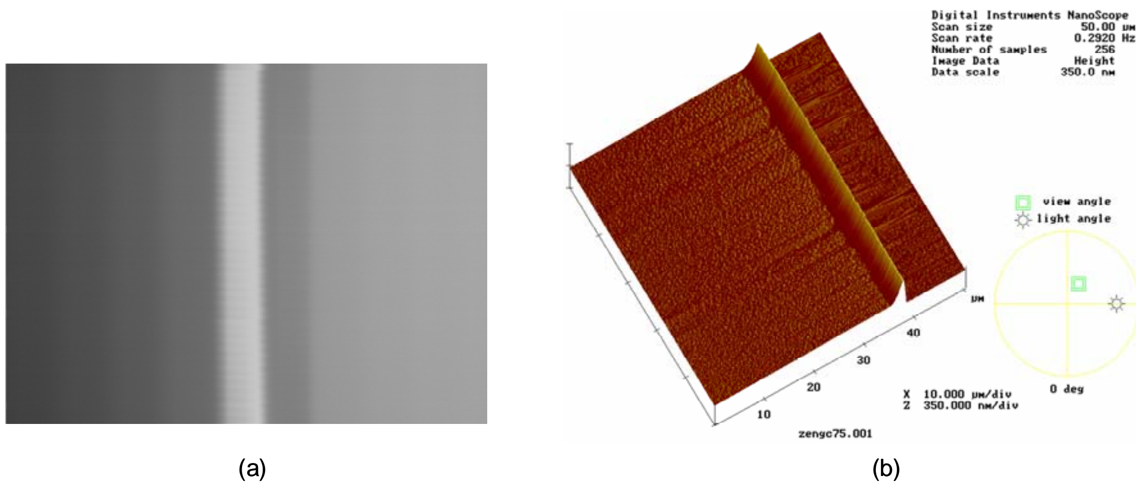

Figure 4: SEM and AFM images of a spacer gate structure. (a) SEM image. (b) AFM image. The structure measures 200±25 nm.

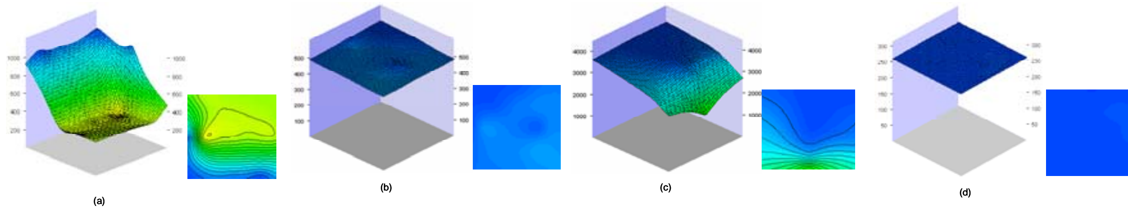

Figure 5: Reconstructions of several thin film surfaces. (a) Polysilicon before uniformity optimization (54% variation). (b) Polysilicon after uniformity optimization (2.6% variation). (c) Silicon nitride before uniformity optimization (20% variation). (d) Silicon nitride after uniformity optimization (0.6% variaiton). The units shown are Angstroms.

fabrication, it certainly cannot succeed if the films vary significantly in thickness over their surfaces. Other relevant process properties can be tailored later by making more minor modifications to the process parameters, but the ability to deposit and etch films uniformly is a prerequisite for attempting to fabricate any sub-100 nm spacer gate structure. Figure 5 shows a comparison of several thin film surfaces. The polysilicon film in fig. 5(a) was grown before optimizing the deposition uniformity, while the polysilicon film in fig. 5(b) was deposited after uniformity optimization. The standard deviation of the thickness over the surface of the film shown in fig. 5(a) is 320 Å (54%). Not only is such variation unacceptable for a single process, this error propagates throughout the entire sequence of deposition process, resulting in an extraordinarily non-uniform film. Following the RIE processes on such a non-uniform sample, the spacers are very likely to vanish altogether. In fact, this phenomenon was observed during experiments. Any attempt to fabricate a spacer gate structure using the film in fig. 5(a) simply would fail. The film shown in fig. 5(b), however, is quite uniform and provides a good starting point for the overall fabrication process. The standard deviation of the thickness over the surface of this film is only 13 Å (2.6%). Similar results have been obtained for SiO_2 and Si_3N_4 film depositions, as have results regarding the reactive ion etching of polysilicon, SiO_2 and Si_3N_4 films.

Composition control is also of principle importance. Thus, currently it is necessary to investigate film composition by using XPS or a similar chemical analysis technique in order to determine the source of the material contamination and to fully optimize these films. With these processes in place, transfer to a GaN based FET is the next logical step.

Conclusions

A method by which sub-100 nm features can be fabricated using only conventional semiconductor processing and optical lithography techniques was exercised. This methodology uses no e-beam in the process but has the potential to create lithographically located features sizes at dimensions approaching 5 nm. Initial results produced a typical gate length of 0.2µm with a high degree of variability. The successful process becomes an exercise in thin film process control, rather than lithography process control. A diagnosis of lack of process control was determined. Each process was systematically improved to bring the entire process under control.

Acknowledgement

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