

# Advances In Processing of Compound Semiconductor Substrates

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## **Abstract**

Compound semiconductor materials such as GaAs and InP have distinct advantages over the more traditional silicon, chief of which is the greater electron mobility within the substrate, allowing greater use in low-noise, high gain applications. However, the advantages of these materials come with corresponding disadvantages. As these materials become attractive for high power applications, they become less suited for one of the major byproducts of this application – heat. In contrast to silicon, these materials have a much lower thermal conductivity, which leads to the primary method of heat management – wafer thinning.

In order to manage the heat, these materials will first be thinned (to minimize the overall thermal resistance), and then patterned with backside metallized vias [1], which serve both as heat sinks, and as a grounding back plane for the circuitry of the device.

This paper discusses recent advances in production technologies intended to address the challenges presented by this process, and allow for high yield manufacturing. First, the challenge of handling these fragile thinned substrates for the required post thinning processes of lithography, etch, and metallization will be discussed. Then, advances in lithography technologies for the alignment and patterning of the vias will be explored. Finally, new processes for compound semi technologies – spray coating and plasma assisted direct wafer bonding – will be presented.

## **Substrate Handling**

The process of thinning of the compound semiconductor wafer presents an enormous challenge to the overall production of devices on these materials, since the materials themselves are extremely fragile (much more so than silicon). Without special handling, it is difficult for the material to survive the thinning process, much less subsequent processing steps.

In order to successfully thin and process these substrates, they must first be mounted onto a rigid carrier. However, since ultimately, the devices will need to be packaged in their thinned form (to retain the newly achieved heat management properties), it is necessary to perform the mounting in such a manner as to be able to remove the carrier at a later point.

In the past, this process would use wax. The benefit was that, by elevating the temperature, the overall adhesion of the wax would decrease drastically, allowing removal of the substrates with very little applied force. Challenges with this method are that, once the substrate has been removed, the residual wax would need to be removed via a solvent cleaning process, which is quite hazardous to the thinned and fragile substrate. In addition, removal of the substrate was frequently performed by human hand, again leading to yield losses.

A new system has been developed which, although it can be designed to process waxes, finds its full advantage using a different adhesion technology - that of double sided thermal release tapes (Figure 1). The system integrates all steps used to perform the mounting of the compound semiconductor wafer onto the carrier. In order to accomplish this, the system will simultaneously process both the carrier substrate and the device substrate through separate steps, with the final result being the bonded pair, suitable for thinning and further processing.



Figure 1: Temporary bonding system – EVG850TB

The carrier substrate (typically sapphire) is passed into a lamination station. Within the station, the thermal release tape is precisely cut from a reel to the carrier substrate's dimensions, and the non-thermal adhesive layer is exposed. Then, the tape is optically aligned to the carrier, and applied to the carrier in such a way as to avoid any stress within the film. Finally, the thermal release layer is exposed, and the carrier substrate is transferred from the lamination station to the bonding station.

While the tape is being applied to the carrier, the device wafer is placed into a coating module, so that a layer of polymer can be placed over the active devices on the surface, to prevent any damage during subsequent processing steps. Once this coating is completed, the wafer is passed into a bake station to

cure the layer. Finally, the substrate is cooled and transferred to the bonding station, where it is attached to the carrier substrate. At this point, the stack is ready for thinning.

## **Lithography**

### **Coating**

Once the thinning process is complete (at which point, the device substrate is typically  $<100\ \mu\text{m}$  thick), it is necessary to pattern the backside vias. Although the primary reason for wafer thinning is due to the heat management issue, another, and very important, reason for thinning is related to the lithographic processing of the vias; more specifically, to etch selectivity.

For example, the etch selectivity of GaAs is typically in the range of 5-10:1, meaning that, for every 5-10  $\mu\text{m}$  of GaAs etched,  $\sim 1\ \mu\text{m}$  of the photoresist layer is consumed. For a full thickness substrate ( $\sim 600\ \mu\text{m}$  thick), this means that a resist layer in excess of  $100\ \mu\text{m}$  may be necessary. Although this is achievable, resist thicknesses of that magnitude are typically used in packaging applications for wafer bumps. [2] The thermally resistive properties of the GaAs would make processing of a layer of this thickness difficult, and the minimum features sizes required for the vias would also be an issue.

By thinning to  $100\ \mu\text{m}$ , this requirement is reduced to  $\sim 10 - 20\ \mu\text{m}$ , which is still a considerably thick layer, but much more manageable. Special processing concerns (such as the use of a cover for the coating module) are still recommended to achieve a highly uniform surface for the resist.

### **Backside Alignment/Exposure**

Following the coating process, a backside alignment and exposure step will be performed. The problem is three fold – first, accurate backside alignment is difficult when the alignment keys are effectively beneath the surface of the substrate. Second is that, due to the nature of the thermal release films, some visual interference occurs with the image of the device wafer. Third is that the existence of these carriers obscures the flat/notch feature of the device substrate, making three-dimensional (x, y, and theta) pre-alignment of the substrate difficult.

The third item is the most readily solved, through the adaptation of optical inspection technology to determine the position of the flat/notch through automated topside examination.

The spacing introduced between the patterns of the device wafer and the wafer chuck by the sapphire carrier is an issue due to the nature of the backside alignment process. Because most semiconductor substrates are opaque,

backside alignment can only be accomplished by digitally representing the position of the mask keys prior to loading of the substrate. Since it is a digitized image, its position is fixed to the viewing area of the microscopes. If the microscopes move, the location represented by the digitized image will also move.

This makes refocusing of the microscopes undesirable, since even when the microscopes are moved just for focus changes (i.e., in z), the spindle motion will typically introduce lateral movement as well. If microscope travel is not perfectly perpendicular to the surface being viewed, some “walk”, or lateral movement, of the image will also occur during refocusing.

Instead, it is preferable to use a process where the microscopes do not need to move to perform the alignment. A simple

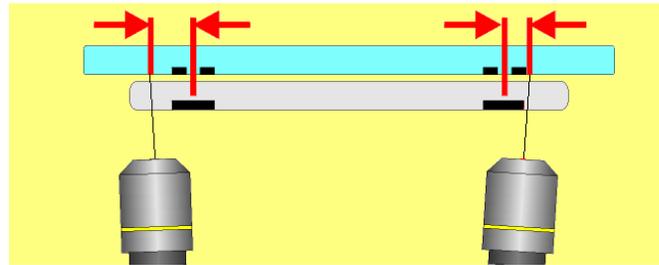


Figure 2: The disadvantages of refocusing

method to do this is to develop an easily defined and referenced focal plane, where the mask and device patterns can be reproducibly introduced. This is done by referencing the two to the top surface of the wafer chuck.

During the digitization process of mask alignment keys, the mask itself is placed into direct contact with the wafer chuck, and the focus of the microscopes is established in that plane. Then, when the mask is lifted, and the wafer inserted in its place (face down - appropriate for backside patterning), the patterns on the face of the wafer, since they are also in contact with the chuck, are also in focus, with no movement of the microscopes.

This is where the problem occurs with carrier-mounted substrates – the carrier prevents contact between the patterns of device wafer and wafer chuck. In the past, a workaround to this process was developed. In this case, a dummy substrate, representing the thickness of the sapphire, would be inserted under the mask. When the optics are focused onto the mask, the focal plane is re-calibrated to account for the thickness of the carrier.

While this process suited to allow alignment of the mounted substrates, especially in a manual manner, it still remained somewhat awkward. Recently, a new process was developed to allow backside alignment of compound semiconductors. The new process utilizes mechanisms already built into the aligner system, it just exploits them in a different manner.

As the name implies, contact/proximity mask aligners are designed to create a very precise separation gap between mask and substrate during exposure. This compound semiconductor

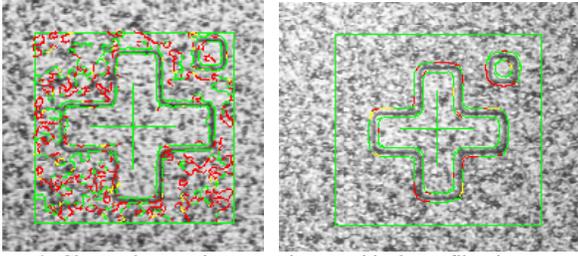


Figure 3: Cluttered vector image vs. image with clutter filtration

backside alignment process makes use of this capability to overcome the difficulties with the carrier. Instead of introducing a mechanical separation through the use of a dummy substrate, the proximity subsystems within the aligner are used to create a pre-defined offset from the chuck to allow calibration of the focal plane.

In this manner, the offset can become a recipe designated value, removing the need to maintain dummy substrates near the exposure tool, including dummies for various sizes/carrier designs. Since the gap is determined using the electronics of the system, rather than a spacer, the process lends itself to much greater degrees of automation.

### Nano-Align

The second issue with the backside alignment process is related to the nature of the thermal tapes themselves. In order to create a near-zero adhesion force upon release, the thermal tapes integrate small capsules within the adhesive film which are designed to rupture at the release temperature. Upon rupture, these chemicals react with the adhesive, such that all reactants are converted to a gaseous product. The problem is that, until rupture, these beads remain visibly within the film, and can conceivably interfere with the automatic recognition of the alignment features, thus preventing automatic alignment of the substrate.

This difficulty is overcome by the recently released alignment enhancement package called Nano-Align. Nano-Align integrates several alignment enhancement features, including improved imaging optics, adaptive, closed loop temperature control, and vector based image recognition, to greatly enhance the alignment capabilities of existing aligner designs.

The vector based image recognition system is the key to overcoming the difficulties with the obscured alignment keys. Rather than simply comparing the gray-scale image on-screen to the memorized gray-scale image, performing a pixel-by-pixel comparison, the vector based system applies intelligence to the image.

It uses gray scale vectors (i.e., shadings from light-to-dark or dark-to-light) to determine feature contours. Each feature is then stored as an object. Since each object has individual values (such as size and position), it is then possible to filter based on these values. In the case of the ob-

scured images, it means that features smaller than a certain threshold (referred to as granularity) can be removed from recognition. Then, only larger scale features are inspected, which are representative of the actual alignment features, thus allowing automation of the alignment process (Figure 3).

However, training of the initial memorized feature can remain an issue as well. The image recognition system provided in the Nano-Align package provides a solution for this as well. Since the recognition is based strictly on contours, it is actually possible to provide a “virtual” alignment key; that is, a key that is simply an electronic image, such as a bitmap. Since this image has none of the clutter or irregularity of one of the actual device keys, it can provide an “ideal” model for comparison.

Additionally, this package allows for simplification of multiple layer alignment key design, because it integrates a “detail feature” recognition routine. This allows recognition, not only of the primary key structure, but also of smaller identifying structures which can be used to indicate layer (see Figure 4).

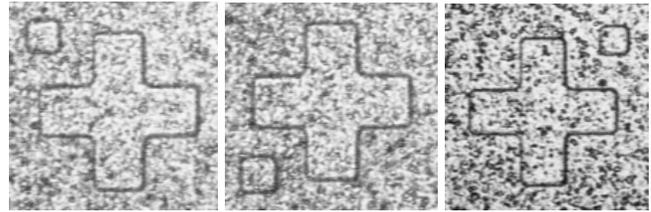


Figure 4: Examples of “Detail Features”

Overall, integration of all of the features available from the Nano-Align package provides for the best possible front-to-back alignment accuracy in the industry, allowing for alignments better than  $1 \mu\text{m}$  at  $3\sigma$  (or,  $0.33 \mu\text{m}$  at  $1\sigma$ ).

Alignment accuracy of this scale can be critical, as the heat transfer capacity of the backside vias is comparable to the size of the via – the larger the via, the more heat removal. However, the size of the via is limited – misplacement can compromise the function of the device. Since Nano-Align allows for more accurate placement of the via, the via can be larger, due to the tighter tolerances between the via and other device structures.

### De-bonding

After all backside processing of the substrate has taken place, the device is typically ready for singulation and packaging. However, before that can occur, the compound substrate needs to be removed from the carrier to which it has been mounted. Unfortunately, this is typically the point of greatest yield loss, as it requires cleaning and handling of this ultra-thin substrate, completely separate from any rigid support. Compounding the problem is that, loss at this point is at its most expensive, since, for all intents and purposes, these are complete and fully functional devices.

With these considerations in mind, de-bonding becomes a very critical step. However, corresponding to the bonding system above, a de-bonding system has been developed which has

a full solution to the handling of these fragile substrate (See Figure 5).

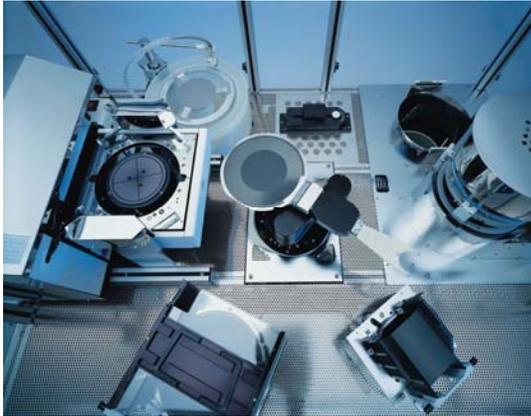


Figure 5 – Debonding Station

Mounted substrates that are loaded to this system will first be placed into a film-frame mounting system. The packaging film-frame will be mounted onto the device side of the stack. Once the film-frame is mounted, the wafer stack is passed into the de-bonding station, where vacuum fixtures will attach to the film frame, and to the sapphire carrier. The temperature of the stack is raised above the release temperature for the thermal release tape, and the device wafer is separated from the sapphire.

Once the device wafer (on film frame) is removed, it is handled to a cleaning station where the protective coat is removed from the device surface. At this point, the device wafer is mounted on the film frame and ready to be delivered for singulation and packaging. At no point during the entire post thinning process was the fragile, thinned compound semiconductor substrate unsupported. In this manner, yield losses have been reduced greatly in the manufacturing of these devices.

### Other Technologies

In addition to the technologies developed for the manufacturing of thinned substrates, additional technologies have been developed to address other portions of the processing of compound semiconductors. First of these is the use of spray coating, especially in the application of air-bridge underfill [3]. The second is the use of plasma-assisted bonding techniques.

A new process has been developed for performing the underfill process for air bridges in power devices, enhancing function by creating protective encapsulation for the fragile structures, and preventing introduction of contaminants that may create an unintended ground. Filling this space can be time consuming and expensive. Spin coating brings distinct disadvantages, as the path from the top of the substrate to the area under the suspended region is relatively small ( $\sim 3 \mu\text{m}$ ), while the structures are suspended 5

$\mu\text{m}$  or more, requiring multiple spin coatings of low viscosity material for proper filling. Spray coating, by contrast, does not rely on radial flow characteristics for material distribution, instead depositing from above, allowing large amounts of low viscosity material to be deposited directly to the substrate. This way, a highly planarized underfill can be provided in a single coating pass, using significantly (90%) less material than spin coating.

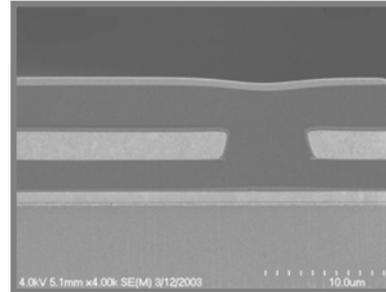


Figure 6 – BCB underfill of air-bridge – courtesy Agilent Technologies

Through the use of plasma activation, direct bonding of wafers can occur with a maximum process temperature of no more than  $350^{\circ}\text{C}$ . By using various gas chemistries, and a variety of RF frequencies, it becomes possible to directly bond all manner of different materials, creating heterogeneous devices that can integrate multiple functions, from the silicon technologies of MEMS and CMOS, to the optical and high frequency technologies of compound semiconductor technologies.

### Conclusion

Cost effective manufacturing of compound semiconductor materials is a critical element of success for companies which process these materials. From the power device industry, to the optoelectronics industry; with strict compound manufacturers and hybrid technologies, yield becomes a major cost model element. Through the introduction of new technologies, product yield can be greatly improved, reducing the overall price per unit of the device, and ensuring the success of manufacturing.

### References

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