Yield Improvement of MESFET Circuits with Idd Ring-Like Pattern

Y.Z. Wang, P. Fowler

ANADIGICS, INC.
141 Mt. Bethel Road, Warren, NJ 07059
Tel: (908) 668-5000, e-mail: ywang@anadigics.com

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ABSTRACT

Diesort yield loss caused by bias current Idd out of specification limits showing a ring-like pattern in our major MESFET products was investigated in this paper. Process splits and DOE were used to identify the root cause of Idd ring-like pattern. It was found that the Idd ring-like pattern was caused by gate gold plating process. The higher plating current density interacting with anode diffuser ring in the plating system resulted in higher stress at the boundary layer in the filter holes. Hence, the stress-induced piezoelectric effect caused Idd shifts to low at these areas.

INTRODUCTION

In our production MESFET process, a bias current measurement, Idd, is often performed at Diesort testing. Some MESFET products have exhibited Idd variations in a ring-like pattern as shown in Figure 1. Depending on the product requirements and process centering, the Idd variations can result in Diesort yield loss because of the bias current out of Diesort specification limits. The yield loss might occur on some wafers in lot, or all wafers in lot. The yield loss on each wafer is about 6-10%. However, even if wafer doesn't have ring-like pattern yield loss, the parametric Idd still shows a ring-like pattern at the lower side of limits. These patterns can consist of as many as 5 rings. Eliminating such systematic, process-generated yield loss is the responsibility of Yield Enhancement. This paper describes how the root cause was diagnosed and fixed. An automated optical defect inspection [1] able to detect a similar ring-like pattern on these wafers has been used in concert with Diesort mapping in the diagnosis and fix.

EXPERIMENTAL

In our MESFET manufacturing, the processes start from bare wafers to implantation and activation, isolation, Ohmic contact formation, "T"-gate formation, and then inactive device formation to Airbridge interconnection and passivation [2]. A schematic drawing of typical MESFET structure is shown in Figure 2. As wafers progress through the process, automated defect inspections are done after certain prescribed operations. The ring-like pattern is first detected after gate process block. A defect map showing ring-like defect pattern from automated defect inspection at gate block is shown in Figure 3. However, it is never seen before Ohmic alloy; those are two consecutive process blocks. This indicates that the ring-like pattern may manifest in the gate process.

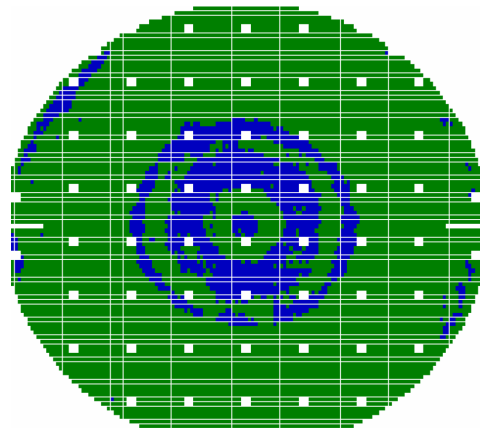

Figure 1. Idd current parameter map showing a ring-like pattern.

Gate formation is a two mask level process. The first mask level defines the FET gate length that is

monitored and controlled. The second mask level facilitates the formation of the plated "T" gate structure. This gate structure is formed by sputtering a base metal and then plating a gold layer in the gate 2 windows. In the first impression the ring-like pattern looks like a tool's footprint. However, the process splits at the tools in gate process didn't show any significant difference by the automated defect inspection. From these process splits in the gate block ring-like pattern was observed on each wafer right after gate gold plating. This indicates that the ring-like pattern may be caused from the gate gold plating.

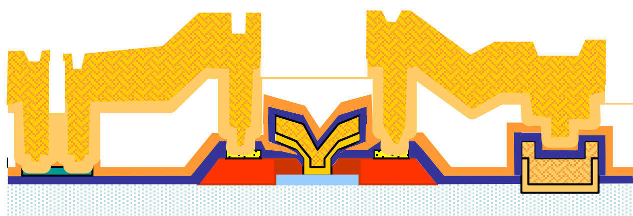

Figure 2. A schematic drawing of typical MESFET structure.

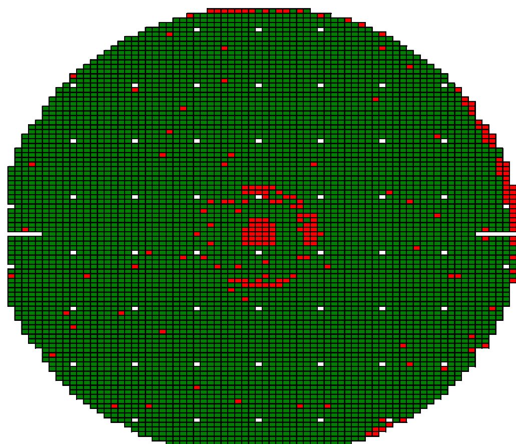

Figure 3. A defect map from automated defect inspection at gate block shows the ring-like defect pattern.

The standard MESFET gate gold plating is performed in a fountain plating system. An additional split was done between the fountain plating system and a bath plating system to determine if the pattern was related to the plating methodology. The wafers processed through the fountain plating system produced clear ring-like patterns. However, no ring-like patterns were observed from the wafers processed in the bath plating system. Although the split showed the difference between two plating systems, it was not clear at that moment whether the pattern is related to system hardware or process parameter setup because these two systems have different hardware as well as different process parameter setup. An experiment was designed to explore the influence of the fountain plater's controlled variables on the ring pattern. The screening DOE included four experimental cells with the condition changes from wafer rotation, gold solution flow rate to plating current density and plating time. The DOE conditions and results are shown in Table 1. It provided the evidence that changing the plating conditions might be a way to eliminate the Idd ring-like pattern. In particular, this DOE indicated that lowering the plating current density and then increasing plating time provided an economic way to eliminate the Idd ring-like pattern.

Table 1. The screening DOE conditions and results

Cell No.	Plating Conditions	Results
Cell 1	0 RPM (no wafer rotation)	Diffuser pattern
Cell 2	33% higher flow rate	Ring pattern
Cell 3	Low current and long time	No ring pattern
Cell 4	Standard	Ring pattern

RESULTS AND DISCUSSIONS

Verification experimental splits were performed at gate plating using standard process versus half current density and double process time. Comparison of automated defect inspect maps and of Diesort Idd wafer maps of all wafers revealed the pattern to be clearly evident on wafers from the standard gate plating cell; the lower Idd current rings occupied ~ 7-8% of wafer. However, the wafers in the cell of half current density and double process time had at most a very slight Idd ring at the wafer center. Figures 4(a) and (b) show the comparison of Idd parameter maps in the standard current density cell versus the half current

density cell. For apple to apple comparison the Idd parameter maps in the figures select Idd range from 20 to 50mA. These splits were repeated and produced the same results. The process using the new plating recipe not only eliminated the ring pattern, thereby reducing the number of low Idd sites, but also showed the significant improvements in other critical parameters. These parameters have very tighter distribution across wafer.

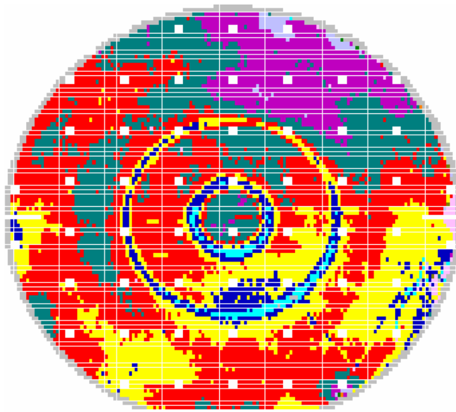

Fig. 4(a)

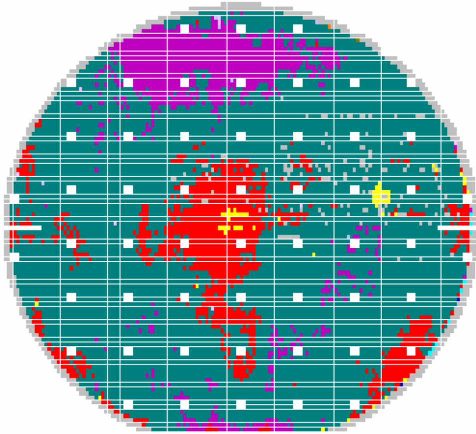

Fig. 4(b)

Figure 4 (a). The Idd parameter map has a ring-like pattern. (b) The Idd parameter map eliminates the ring-like pattern.

Inspection of the wafers split at the gate plating reveals that the wafers with standard gate plating exhibit rough gold at the wafer center and the wafer edge, while the wafers with new gate plating recipe have a more uniformly less textured surface. It is believed that the ring-like pattern was caused by the anode diffuser ring in the plating system. There are some areas that have locally lower gold solution flow because of the filter hole distribution. At high current density the gold solution does not have a chance to replenish itself at the boundary layer in these areas. This can change the deposited gold grains, thickness and thus roughness. Lowering the anode current density allows the gold solution in these areas to replenish and improves the gold grains and across wafer uniformity. This has been verified independently by the gold resistance Rg uniformity across wafer as shown in Figure 5.

The Idd-ring pattern is caused by the properties of the plated gold. Most likely the optically discernable rings are indicative of variations in the plated gold stress. As described before, high plating current density interacting with the anode diffuser rings will result in larger grains at the higher deposition rate. At the same time, the plating induced stress cannot be released and will store in the gold film. Stress induced piezoelectric effect in GaAs MESFETs have been described by Asbeck et al. [3], and subsequently two dimensionally by Lo and Lee [4]. The electrical characteristics of GaAs self-aligned MESFETs depend on the orientation and size of the gate as well as stress conditions in respect to the substrate due to the nature of GaAs zinc-blende crystal structure. Based on their work, our [011] oriented FETs experience a decrease in Gm when there is an increase in compressive stress. The plated gold is compressive. Since Idd is set up by the Vgs applied to the FETs in the circuit path, the decrease in Gm results in a decrease in Idss and therefore lower Idd in the boundary areas of the anode diffuser rings.

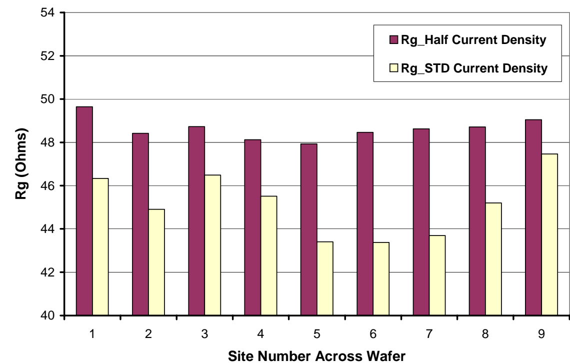

Figure 5. Comparison of gold resistance Rg site average across wafer between standard current density and half current density process.

CONCLUSIONS

In this study, the root cause of Idd ring-like pattern was identified as the gate plating process. The ring-like pattern was caused by the interacting of higher plating current density with anode diffuser ring in the plating system. Stress-induced piezoelectric effect plays an important role in the Idd characteristics of our GaAs short channel self-aligned MESFETs. By adjusting current density and plating time, we are able to eliminate the Idd ring-like pattern, and hence improve the diesort yield. Subsequently, we have improved the uniformity with the introduction of a new diffuser.

ACKNOWLEDGEMENT

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ACRONYMS

MESFET: Metal Semiconductor Field-Effect Transistor

DOE: Design of Experiment

GaAs: Gallium Arsenide