Improving Final Test Yield and Reliability through Backside Final Outgoing Inspection

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Abstract

Implementing an automated frontside final outgoing inspection (FOI) process on power amplifiers is not new.[1] However, until recently technology to automatically inspect backside vias had not been developed, but Compound Semiconductor Fab One (CS1) has implemented a process that can distinguish between visually "good" and visually "bad" backside vias. The importance of implementing an inspection process on the backside vias is crucial in maintaining final test yields and insuring reliable devices are passed along to the final user. This paper presents the benefits of implementing a backside via inspection process.

INTRODUCTION

Backside processing of backside vias on Gallium Arsenide (GaAs) wafers begins after final unit probe testing, in which the good and bad die are "electrical binned " producing a unit probe map. This mapping process indicates which die are electrically good and which are electrically bad.

Wafers that are processed through the backside via process require additional processing steps that include wafer/carrier mount, thinning, backside photo-resist mask definition, backside via etch, wet clean, photo-resist strip, oxygen plasma clean, seed layer deposition, electroplating, demounting the carrier from the wafer and finally die separation.[2]

The processing steps used to manufacture backside vias can have a variety of processing issues including incorrect pattern definition, blocked vias, veils, wet etch/clean defects as well as inadequate metal coverage within the via

Wafers that have been processed through the backside via module cannot easily be tested before final assembly. It is extremely important that a backside via inspection is performed to insure die do not fail in final assembly builds, or worse, in the field!

CS1 has not only demonstrated the ability to perform automated outgoing inspection on the front side of the wafer, but the backside via as well. Implementing a backside via inspection has enabled the process groups to improve the performance of the source vias along with reducing the amount of variation between wafers.

In addition to implementing an automated inspection for the backside vias, this methodology can help address in line excursions, improve cycle time and reduce escapes. It can also result in a significant increase in total FOI yield.

Figure One: Irregular of blocked backside vias

Due to the variation in manufacturing backside vias, any yield enhancement efforts must incorporate a repeatable and accurate monitoring system. In the past, CS1 used a sampling of SEM measurements to determine the health of the backside via. When SEM measurements were taken, only a few die were inspected. This sampling size was not adequate to catch all the defects due to process variations. Defects such as non-etch out areas (NEO), irregular vias (photolithography) or blocked vias could escape which could affect final assembly test yield. An example of such defects are depicted in figure one: Irregular or block backside vias.

With out the ability to electrically test the backside vias a method was needed to visually inspect them. With an automated back via inspection it is possible to visually inspect every via on every wafer, thus quantifying the amount of device hindering defects.

BENEFITS OF IMPLEMENTING AN AUTOMATED INSPECTION SYSTEM

First, it is useful to understand the configuration of the inspected wafer. Front side processing (integrated circuit) is created on a GaAs wafer, the wafer is then mounted to a sapphire carrier and the backside thinned. Next, the backside vias are defined using a photoresist process and the backside vias etched to the desired depth. This provides the ability contact the front side contacts.

During this etch process, veils are formed (a better explanation of veil formation is given by Campbell, Fender,

Daly and Costello, 2005) and must be cleaned out, which is difficult due to the depth of backside via. This stripping/cleaning step is a wet process. If the backside vias are not cleaned properly, then the subsequent metalization can have adhesion issues which can lead to reliability failures. The intent of the backside inspection is to find defects in the backside vias prior to metalization.

Due to backside processing there is the possibility for via defects such as missing vias, vias not etched out (NEO), veils or GaAs residual left in the vias to occur. Because there is not an in-line method for testing backside via defects, it became a priority that a system to visually inspect the backside via be develop.

The importance of backside via inspection has been to catch defects that could possibly alter final assembly yields. In addition, it provides a method to monitor excursions in the backside via processing. Implementing an automated inspection for backside vias has also provided a method for the process groups to quantify process changes and gauge process improvements. These improvements are part of a continuous improvement program (CIP) that CS1 uses to track and prioritize process improvement activities.

TOOL DESCRIPTION

Currently CS1 uses an automated inspection system for Final Outgoing Inspection (FOI) system, which can inspect the front side as well as the backside of the wafer. These tools utilize high quality objectives. This tool was set up to inspect electrically good die from an imported unit probe map. Once the map is imported into the inspection tool the die are then inspected for visual defects using variations in reflected light. These variations are identified by comparing a reference image to an inspected die. The reference image is created by training in many visually good die. These die are then merged together to create a mean image and a standard deviation image. The mean image is used to compare to the inspected die while the deviation image used to determine if a die is acceptable based on the gray scale sensitivity levels. These variations in light are in the gray scale of 0-255, black-white respectively.

For the front side inspection, this system has many features to align to per die. With the backside inspection the only feature on the die to align to are the backside vias. In order for the system to align to the backside vias, the drift had to be set low and the illumination reduced to catch the slight differences in color variations. Since the size of the backside vias and thus defects were an issue, the filter reduction factor was set to zero. This allowed the system to catch the smallest of defects with in the backside vias.

TOOL LIMITATIONS

The challenge in implementing a backside via automated optical inspection system lies in setting up a tool to accept variations in a die while rejecting true defects. Therefore sustaining the inspection system requires an important balance between minimizing over rejection and minimizing escapes. Due to process induced variations in the surface roughness of the back via, there is a high risk of over rejection. Although rough gold passes defect specification, the system may reject die with rough gold if the inspection system was trained to another wafer in the lot that may have smooth gold. To prevent this, an out of control action plan was established. If an operator finds that die have been incorrectly rejected, they will retrain the reference image to include rough gold. The chart below shows how the variation in dark gold can alter the source via yields.

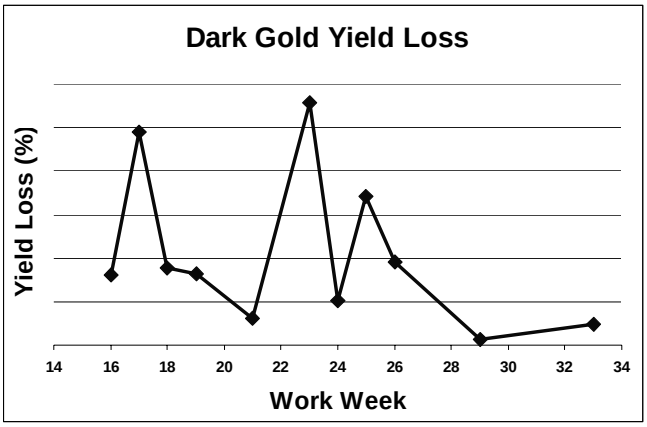

Figure Two: Dark gold yield loss on test runs.

Another threat of over rejection with this system is posed by particles on the backside of the wafer. The tool uses a set of exclusion areas to block out areas of the wafer not inspected. For the backside via inspection the only area of concern for inspections are the backside vias. The software limits exclusion areas to squares and circles (an example of exclusion areas are exhibited in figure four: exclusion areas around the backside vias). Due to the limitations in exclusion areas not reaching the exact perimeter of the backside vias there is the potential of over rejection

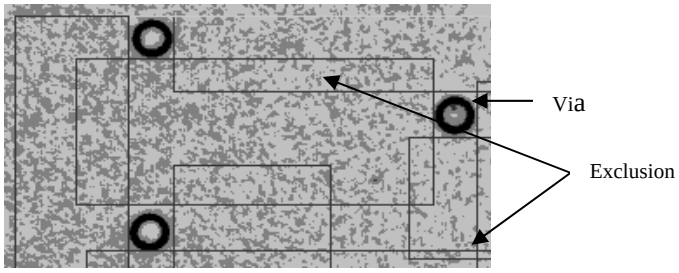

Figure Three: Exclusion areas around the vias.

DATA COLLECTION AND ANALYSIS

For on product measurements (front side defectivity) data is collected, computed and categorized to provide information to the process groups for future yield enhancement. Once the data is collected a sample of the defects are categorized using the visual aids provided. The number of defects categorized is dependant upon the amount of die rejected. This data is then put into a formula to determine the yield loss for each specific category. This formula is weighed to show defects that might only affect one or two wafers. Figure four bubble defect shows how this weighed calculation caught an increase in bubble defects. This methodology has assisted the process groups determine a root cause in numerous occasions.

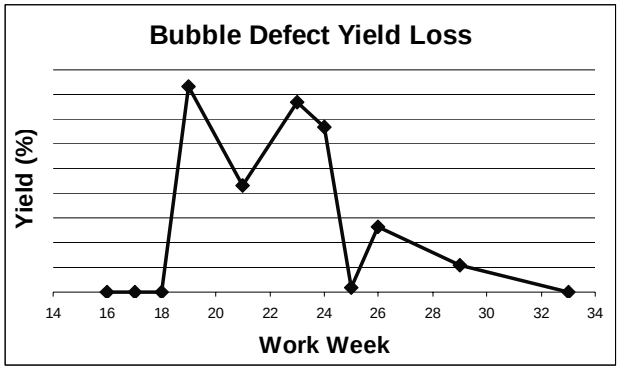

Figure Four: Bubble defect yield loss trend chart.

Along with tracking yield data on product, the backside via inspection process has been instrumental for backside via process improvement experiments. The backside via process had been experiencing some yield loss at final test and through cross-sectional analysis, it was determined that one of the causes was due to insufficient cleans.[3] The wets process engineers used the back via inspection process as the main method to determine the appropriate clean needed for the source via process. This saved both time and money in reducing the amount of SEM's needed per sample. In the figure five: (yield data for cleans test) yield improvement with the new cleans is depicted.

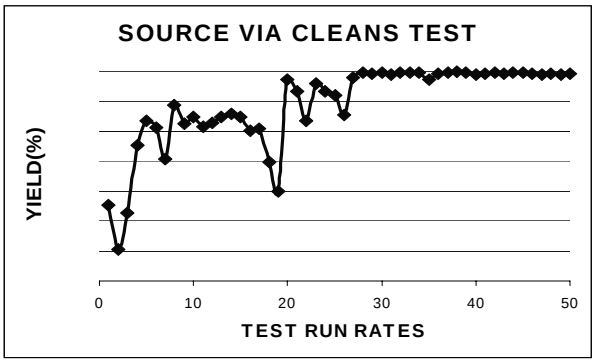

Figure Five: Yield data for cleans test

CONCLUSION

Since there is no easy method to electrically test the backside via, backside inspection is the best quantitative method to determine yield loss and shifts in the backside via process. This methodology not only monitors the product line but also helps address inline excursions, improve cycle time and reduce escapes that could impact final test yields. CS1 has demonstrated the ability to inspect backside vias

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ACRONYMS