

0.15 μm Power pHEMT Manufacturing Technology for Ka- and Q- Band MMIC Power Amplifiers

Sabyasachi Nayak, Ming-Yih Kao, Aimee Bross, Shuoqi Chen, Qinghui Wang, Sean Hillyard, Andrew Ketterson, Kenneth Decker, Joseph Delaney, and Keith Salzman

TriQuint Semiconductor, Richardson, TX 75080 USA, SNAYAK@TQTX.COM

KEYWORDS: POWER AMPLIFIER, GaAs, PHEMT, MMIC, KA-BAND, Q-BAND, MILLIMETER-WAVE.

ABSTRACT

TriQuint Semiconductor, Texas has developed a very reproducible, high yield, and high reliability, 0.15 μm power pHEMT technology with state-of-the-art power performance of MMIC PAs for Ka- to Q- band. Careful design of epitaxial structures and optimization of critical processing steps have achieved high performance and high yield. Using this technology, a compact 2W MMIC at 32-38 GHz (TGA4516, 4-mil), 3.5W MMIC at 35 GHz (TGA4517, 2-mil) and 2W MMIC at 45 GHz (TGA4046, 4 mil) have been designed and produced. In this paper, we report our fabrication process, device characteristics and MMIC RF performance at Ka- and Q- band.

I. INTRODUCTION

High power and high efficiency MMIC power amplifiers at Ka- and Q- band are critical to both the commercial wireless application such as VSAT and the advanced military millimeter-wave (mm-wave) systems for communication and phased array radar applications [1]. Over the years, extensive effort has been made to realize a low cost manufacturable technology for Watt level MMIC power amplifiers at high frequency [2-5]. To achieve high power and high performance MMICs over these frequency bands, the essential requirements are small chip size, high gain, and high output power density per unit cell, high linearity and efficiency. Therefore, it is very important to develop a process technology to meet those high standards, and, at the same time low cost manufacturable process with high yield and high reliability. At TriQuint Semiconductor, Texas, we have developed a process technology, which meets the requirement for a mm-wave technology and very suitable for realizing high frequency MMIC power amplifiers.

Based on our well-established double recess 0.25 μm pHEMT and single recess 0.15 μm pHEMT processes, we have developed a double recess 0.15 μm power pHEMT process for mm-wave application. Device epitaxial structure and fabrication process have been optimized to meet the requirement for mm-wave technology. In this paper, we report the fabrication process; device characteristics and MMIC RF performance based on this mature high performance technology.

II. 0.15 μm POWER PHEMT MMIC TECHNOLOGY

A. EPITAXIAL STRUCTURE

The device structure used for 0.15 μm power pHEMT is a double hetero-junction epitaxial structure grown by molecular beam epitaxy (MBE) on a semi-insulating GaAs substrate. The epitaxial structure is optimized to a maximum drain bias of 6V. The layers grown on top of this substrate are, semi-insulating GaAs buffer, AlAs/GaAs superlattice buffer, AlGaAs spacer layer, InGaAs channel layer, AlGaAs spacer layer, n- AlGaAs donor layer and n+ GaAs cap ohmic contact layer. A 15 \AA AlAs etch stop layer is inserted in the AlGaAs donor layer to consistently maintain the height of Schottky junction with respect to channel to achieve desired pinch-off voltage and transconductance. In addition, two silicon planar doping layers are inserted on both sides AlGaAs (spacer)/-InGaAs-(channel) / AlGaAs (spacer) to increase the current capability of the channel. Hall measurements produced a sheet carrier concentration of $3.2 \times 10^{12} \text{ cm}^{-2}$ with a room temperature mobility of $6500 \text{ cm}^2/\text{V.s}$

B. FABRICATION PROCESS

0.15 μm power PHEMT fabrication process begins with the deposition of ohmic contact to create source, drain and all the pads and other geometries. Source to drain spacing is set to 2 μm . After ohmic contacts, isolation implant is performed to isolate active areas from the field areas of the device. This is followed by the wide recess lithography using e-beam. In wide recess steps, a dry plasma etch is used to remove the n+ GaAs cap layer and wet process is used to trim the AlGaAs spacer layer to a desired saturated (I_{sat}) current target. This is followed by an e-beam lithography to define the 0.15 μm T-gates using bilayer resist profile. The T-gate is centered within the wide recess, which is already centered within the source and drain. After the T-gate lithography, gate recess is performed followed by Ti-Pt-Au metallization to form the Schottky junction. Gate metal is lifted off from other areas. The channels are passivated by using low k dielectric immediately following the gate metallization. This is followed by silicon nitride passivation.

Other MMIC components, fabricated on the front side processing include, TaN resistor and 3 levels of metal interconnect (3MI) including Au plated airbridge and 3 types of SiN capacitor and a SiN protective overcoat. After the front side processing, the substrates are thinned down to either 2 mil or 4 mil, followed by via hole formation by etching the backside and backside metallization using Au.

C. IN-LINE PROCESS CONTROL

Several critical process parameters, i.e. CD sizes of wide recess, trunk and cap size of T-gates, Isat at wide and narrow recess steps are measured and tracked and tracked using statistical process control (SPC) charts. In addition, we perform automated electrical measurements on process control monitor (PCM) and test structures at three different stages of the front side processing. Critical parameters such as, Idss, I_{max}, V_p, BVGD, BVGS, G_mmax, R_d, R_s, R_g, ohmic contact resistance and resistance of gate metal stack, capacitance of capacitors are measured and monitored using trend charts. Figure 1 shows the wafer mean V_p plot of 74 wafers of this technology.

In addition to critical process and DC parameters, equivalent circuit parameters of a standard FET cell (SFC, 4X75 μm finger, 15 sites per wafer) are monitored on each wafer. Small signal RF measurements were performed on the SFC over frequencies of 0.5-26 GHz. Equivalent circuit parameters (ECPs) are extracted using the analytical model discussed by Campbell and Brown [6]. Figure 2 shows the trend of the cut off frequency, f_T , of 74 wafers.

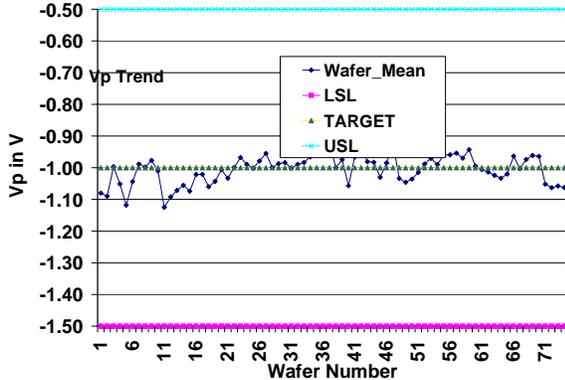


Figure 1. Wafer mean pinch-off voltage of 74 wafers.

III. DEVICE CHARACTERISTICS

Fig. 3 shows G_m transfer curve and drain current I_{ds} vs V_{gs} at V_d = 6V. This data is taken from a 4X75 μm unit FET cell and normalized. It represents a typical characteristic of the 0.15 μm power PHEMT process. It is important to note that the 2 terminal gate to drain

breakdown voltage of this device is -13V to -14V with I_{max} of 680 mA/mm. This gate to drain breakdown provides sufficient margin for the device operation at V_d = 6V bias condition. Load-pull measurements are done in our engineering lab on selected samples at V_d=6V and I_d=100 mA/mm. At 40 GHz load-pull measurement of 400 μm FET cell (10x40 μm), demonstrated the output power density of 815 mW/mm with 40% PAE. Table I summarized the key performance of this process.

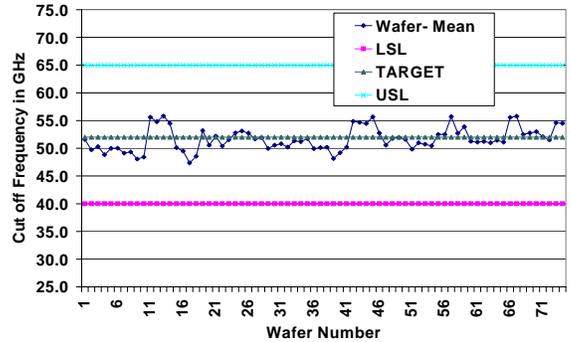


Figure 2. Wafer mean cut off frequency (f_T) of 74 wafers.

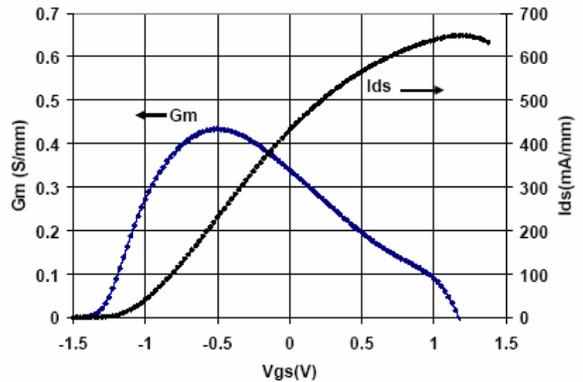


Fig. 3. Transconductance (G_m) and drain current (I_{ds}) vs gate to source voltage (V_{gs}).

TABLE I. THE KEY PERFORMANCE OF TRIQUINT'S 0.15 μm POWER PHEMT TECHNOLOGY

Parameter	Unit	Nominal Value
I _{dss} (V _{gs} =0)	mA/mm	375
I _{max} (V _{gs} =1.5V)	mA/mm	680
G _m	mS/mm	475
V _p	V	-1.0
BVG _D	V	-13
F _t @ 5V, 100mA/mm	GHz	52
F _{max} @ 5V, 100mA/mm	GHz	150
P _{out} @ 40GHz, 6V, 100mA/mm	mW/mm	815
PAE @ 40GHz, 6V, 100mA/mm	%	40
Interconnection	N/A	3MI
Substrate	μm	50 & 100

IV MMIC PERFORMANCE AND YIELD

Using this 0.15 μm pHEMT process, we have designed Ka/Q-band MMIC power amplifier. The design of the amplifiers started with an accurate small signal FET model, which was extracted from broadband S-parameter measurement on selected FET cells. The optimum power load, evaluated from load pull power measurement, was utilized to design the desired load target. Details of the design of two MMIC power amplifiers, TGA4516, 2W at 32-38 GHz [7] and TGA4046, 2W at 45 GHz [8] are discussed elsewhere. MMIC power amplifiers are fabricated on a 100 μm thick GaAs substrate with via at the end of source pads of the device. DC and RF parametric yield of higher than 80 and 90% respectively.

MMIC power amplifier, TGA4516-EPU, presented herein consists of three amplification stages with the following gate peripheries: 4x400 μm FET cells at the 1st stage, 8x320 μm at the 2nd stage and 8x520 μm at the output stage. The MMIC was very compact design with a die size of 6.46 mm^2 (2.790 mm x 2.315 mm) and the total output FET periphery was 4.16 mm. MMIC dies were tested on wafer at the RF probe in CW mode for small signal gain and pulsed mode for output power probe. Selected MMICs were mounted on CuMo carrier plate for fixture evaluation. The data shown here are on wafer and the fixtured results.

Fig. 4 shows the typical small signal response of the MMIC HPA at the fixture test. The measured small signal gain is typically 20 dB from 33 to 36GHz. The maximum in-band input and output return losses are 5dB. Over 32–38 GHz, the HPA exhibit 16 to 20 dB of gain. On wafer probe of MMICs are done at reduced bias condition to minimize the thermal impact environment. Figure 5 shows the plot of the wafer median S21 (400 dies/wafer) of 20

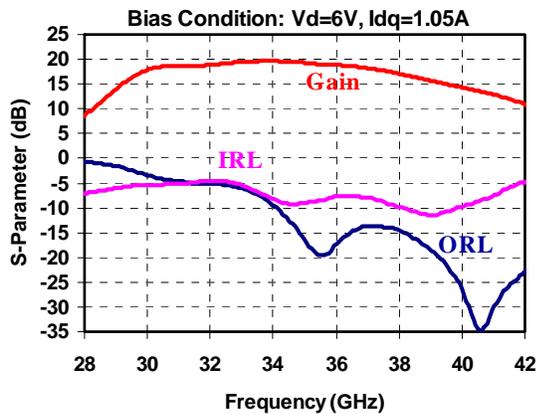


Fig.4. Measured small signal S-parameters of the MMIC TGA4516 HPA at $V_{ds} = 6\text{V}$ and $I_{ds} = 1050\text{mA}$.

wafers probed at RF probe. Median small signal gain varies by 1 dB from one wafer to the other. Variation within a wafer is about 1 dB.

The typical saturated power (P_{sat}) and P_{1dB} output power performance is shown in Fig. 6. Average 33 dBm (2 Watts) saturated output power was demonstrated over a range of frequency of 32 to 38 GHz. The peak P_{sat} in this frequency range reaches 34 dBm (2.5 Watts) with 25% PAE. This HPA demonstrated 604 mW/mm² output power density on its output FETs and 389 mW/mm² power density for a single MMIC chip. This HPA exhibited excellent high band edge RF performance, P_{sat} of 32 dBm, P_{1dB} of 31 dBm over a frequency range of 37 to 38 GHz.

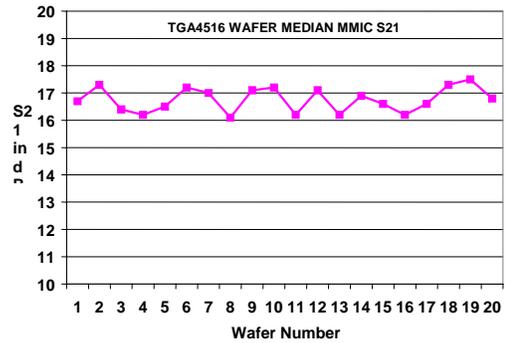


Figure 5. Plot of wafer Median S21 in dB TGA4516 MMIC at 35 GHz. MMICs.

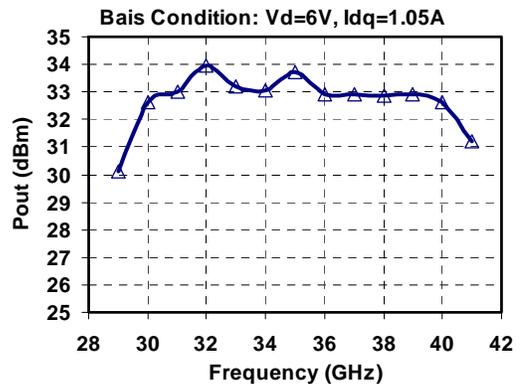


Fig. 6. Measured saturated output power of MMIC (TGA4516-EPU). Test condition: $V_{ds} = 6\text{V}$, $I_{dsq} = 1050\text{mA}$.

MMIC amplifier, TGA4046, 2W at 45 GHz, is designed using a balanced approach in order to avoid phase imbalance problem associated with large gate periphery amplifier at high frequency. Lange couplers were used to form the balanced configuration. The total gate periphery was 12.8 mm with a die size of 14.62 mm^2 (3.4 mm X 4.3 mm). Each half of the amplifier consists of 3 stages with drive ratio of 1:2:2 (1280, 2560 and 2560 μm). In order to minimize the thermal effects, MMIC are on-wafer tested at

a reduced bias condition at RF probe at $V_d=4V$ and $I_d=2A$. In fixtured environment with good thermal contact, all RF tests are done at full bias condition, $V_d=6V$ and $I_d=2A$. Figure 7. shows the measured small signal gain of the amplifier vs frequency. Gain is 16 dB at 44 and 45 Hz and more than 15 dB from 42-46 GHz. Input and output return loss are between -10 to -15 dB. Figure 7 shows the spread of small signal gain across 6 wafers in a lot. At 45 GHz, the spread within a wafer is around 1.5 dB with a wafer-median spread of 1dB across a lot. The smaller spread of RF performance shows the robustness of the process with respect to manufacturability. Power tests are performed under the CW drive. Figure 8 shows the power performance of 12 dies (2 dies per wafer in a 6-wafer lot) over the frequency band of 40 and 48 GHz. Output power of TGA4046 is higher than 33.5 dBm at the designed operation of 44-46 GHz, an equivalent of 437 mW/mm per FET periphery. PAE of the MMIC is around 14% at $P_{in}=20$ dBm. This Q-band MMIC demonstrated higher gain and output power performance compared to the published results [2-4].

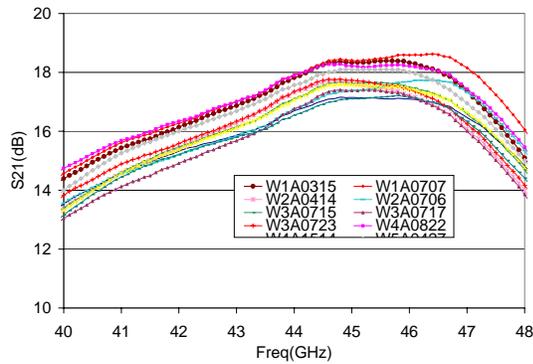


Figure 7. Measured small signal gain of the 12 dies from 6 wafers vs frequency (TGA4046) at $V_{ds} = 6V$, $I_{ds} = 2A$.

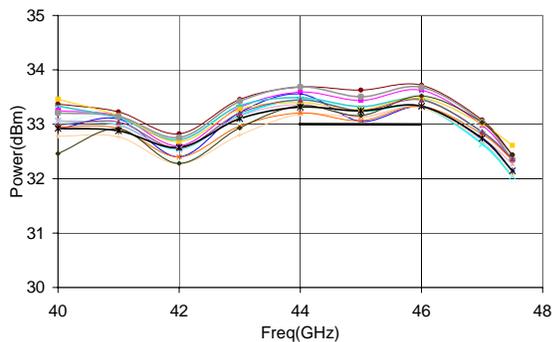


Figure 8. Measured saturated output power of 12 dies from 6 wafers vs frequency of 2W MMIC HPA, $V_{ds} = 6V$, $I_{ds} = 2A$ TGA4046.

V. RELIABILITY

A complete three-temperature reliability study was done on 6 X50 μm pHEMT unit cells to extract the activation energy to calculate the median lifetime of the circuits at the actual operating temperature. An extensive thermal modeling based on device geometry was done to calculate the rise in channel temperature from the base plate temperature. Samples are selected from two different lots (10 wafers) to capture any inherent process variations with time. The median lifetime (t_{50}) values were extracted from the log normal distributions of the lifetime of devices. Arrhenius plot of median lifetimes versus the channel temperature of 296, 281 and 266 $^{\circ}C$ was used to extract the activation energy of 1.7 eV with a lifetime of 1E7 hours at the channel temperature of 140 $^{\circ}C$. A single temperature reliability test is performed on 3 samples from each wafer to ensure the reliability of this technology.

VI. CONCLUSION

In this paper, we have demonstrated a high performance, reproducible, high reliability manufacturing technology for Ka- to Q- band MMIC power amplifiers operating at the drain bias of 6V. Using this technology, we believe that we have produced MMIC PAs with best output power and power density operating at Ka- to Q- band. We attribute the state-of-the-art performance of this technology to the combination of design of epitaxial structure, 0.15 μm MMIC processing techniques with excellent process control, and the millimeter-wave circuit design capability.

REFERENCES

- [1] G.E. Brehm et al., "Commercial Application of GaAs Millimeter Wave MMICs," 2004 Compound Semiconductor Manufacturing Technology Conference, pp.-28-31.
- [2] S.J. Nash et al., "A 1.4W Q-Band GaAs PHEMT MMIC," 1997 GaAs IC Symposium, pp. 283-286.
- [3] T.H. Chen et al., "One Watt Q-Band Class A Pseudomorphic HMET MMIC Amplifiers," 1994 IEEE MTT-S Int. Microwave Symposium. Dig., pp. 805-808.
- [4] C.F. Campbell and S.A. Brown, "A Compact 40 GHz 0.5-Watt Power Amplifier MMIC," 1999 IEEE GaAs IC Symp. Dig., pp.141-143.
- [5] K. Kong et al., "A Compact 30GHz MMIC High Power Amplifier (3W CW) in Chip and Package Form," 2002 IEEE GaAs IC Symposium Dig., pp. 37 – 39, 2002.
- [6] C.F. Campbell and S.A. Brown, "An Analytic Method to Determine GaAs FET Parasitic Inductances and Drain Resistance under Active Bias Condition," 2001 IEEE Transaction of Microwave Theory and Techniques, pp-1241-1247.
- [7] S. Chen et al., " A Ka/Q Band 2Watt MMIC Power Amplifier Using Dual Recess 0.15 mm PHEMT Process," 2004 IEEE MTT-S Digest, pp. 1669-1672.
- [8] Q.H. Wang et al., " A High Power Q-Band MMIC Power Amplifier Based on Dual-Recess 0.15 μm pHEMT," 2004 IEEE CSIC Symposium, pp. 133-136.