# Development of L-band 28V Operation GaAs FET and Optimization for Mass Production

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**Abstract**

**We have developed L-band FET for 28 V operation and succeeded its mass-production. A main feature of the FET structure is the asymmetrically extended (gamma-shaped) gate. By controlling the deviation of gate fabrication process within 0.1 μm, the high repeatability is achieved. The average BVgdo of 80.5 V with a standard deviation of 1.4 V are obtained both within lots and across wafer runs. The developed high power push-pull FET achieves 250 W(54 dBm) output power, 15.5 dB linear gain and 25 % drain efficiency at 2.14 GHz. In addition, the device shows excellent reliability with estimated MTTF of greater than 4x10$^6$hours at Tch of 145 deg-C.**

## INTRODUCTION

A high output power amplifier is strongly required in modern wireless-communication systems. There are two approaches to achieve the higher output power; increasing the drain current, and increasing the operation voltage. The former approach has been commonly employed in the GaAs FET technology, and the output power level of 300 W was achieved by increasing the gate width [1]. But the higher voltage operation is preferable for the following reasons;

1) The power density is increased.
2) The matching circuit loss is reduced.
3) The power gain is increased and the linearity can be improved.

Thus, we set the target of the operation voltage to 28 V, which is commonly employed in LDMOS technology, and successfully developed the GaAs FET, featured with the asymmetric gate electrode. This paper describes optimization for mass production, production repeatability, performance, and reliability of the developed 28 V GaAs FET.

## FET STRUCTURE

Figure 1 shows the schematic cross section of the developed FET structure. In this work, Si doped GaAs channel layer, AlGaAs Schottky layer and a WSi/Au gate were employed. The asymmetrically extended (gamma-shaped) gate electrode relaxes the electric field around the gate electrode. The overhanging length (Lh) and the gate-to-drain distance (Lgd) are the key parameters to improve the gate-to-drain breakdown voltage (BVgdo). The optimum values of the Lh and Lgd were examined in the view of not only the performance but also the mass-production repeatability.

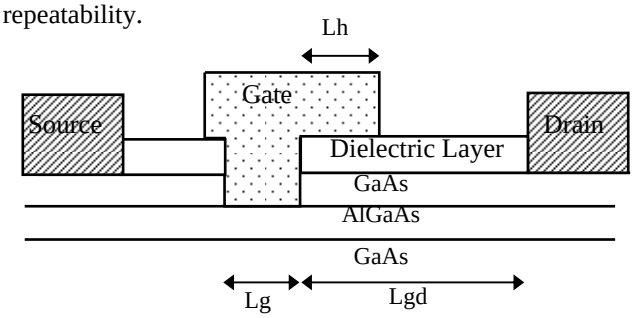


*Fig.1. Schematic cross-sectional view of developed FET*

## OPTIMIZATION FOR MASS PRODUCTION

### *a. The overhanging length (Lh)*

The BVgdo degradation at high temperature can cause thermal runaway, which used to be one of the major problems of the high power GaAs FET. The gamma-shaped gate contributes to maintain the BVgdo high even in high temperature range. Figure 2 shows the BVgdo dependence of Lh and temperature.

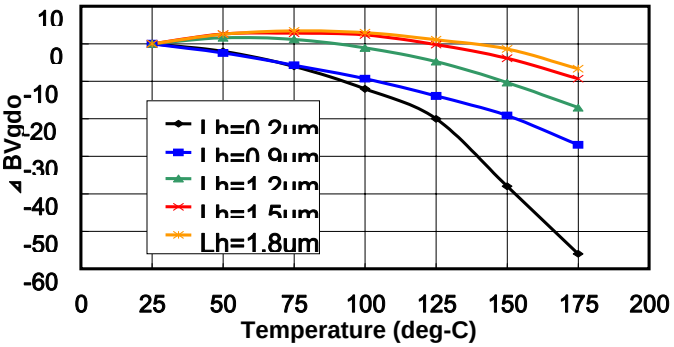


*Fig.2.* Δ BVgdo dependence of Lh and temperature.

To keep the adequate BVgdo level even at 175 deg-C, which is our targeted maximum channel temperature, the Lh is required to set longer than 1.4 µm. On the other hand, the gate-drain feedback capacitance (Cgd) is in proportion to the Lh, and which causes gain reduction. Figure 3 shows the ΔGsmax dependence of Lh. The degradation-rate of Gsmax is estimated 0.13 dB/µm around Lh=1.5 µm.

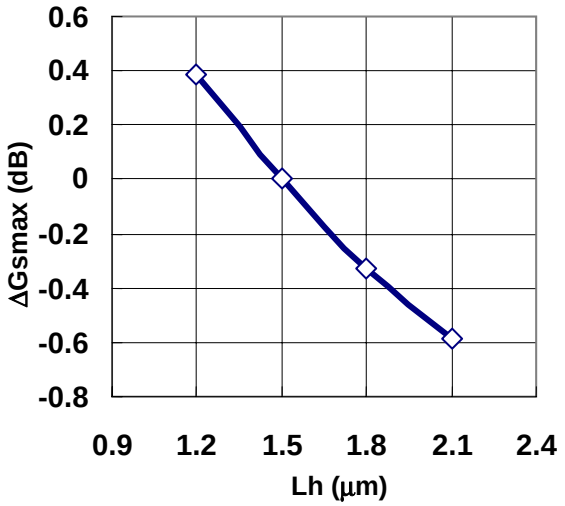


*Fig.3.* Gsmax vs Lgd @2.1 GHz

The actual Lh is determined by not only designed length but also the alignment accuracy of the buried gate fabrication process and the over gate fabrication process. Therefore, we control this alignment deviation within 0.1 µm and set the Lh to 1.5 µm, which ensures that Lh is longer than 1.4um even in the lower limit. In addition, the gain deviation, generated by this miss alignment, is less than 0.2 dB.

***b. the gate-to-drain distance (Lgd)***

The Lgd also affects the BVgdo. Figure 4 shows the BVgdo dependence of Lgd.

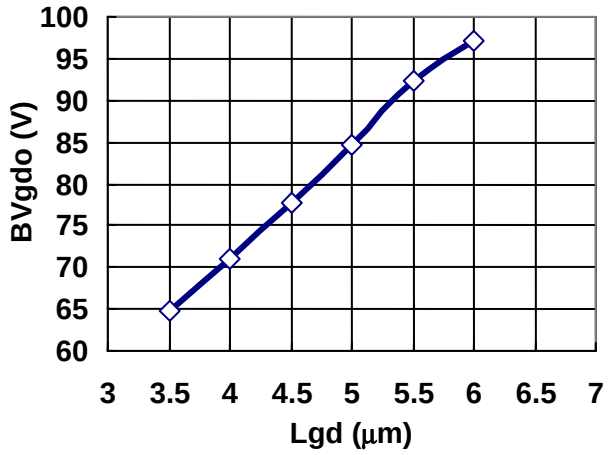


*Fig.4.* BVgdo vs Lgd @Lh=1.5 µm.

The rate is estimated 12 V/µm. The deviation of the Lgd is originated from the alignment of the ohmic metalization process and the gate electrode process. As no significant trade-off exists in Lgd in the sub-micron order, the conventional alignment rule of ±0.2 µm was adopted and the Lgd was set to 5.0 µm to obtain the required BVgdo level.

## REPEATABILITY

Figure 5(a)~(c) show the distribution of on-wafer test data with 90 W FET (Wg=133.1 mm) from multiple wafers among multiple wafer lots in actual mass-production.

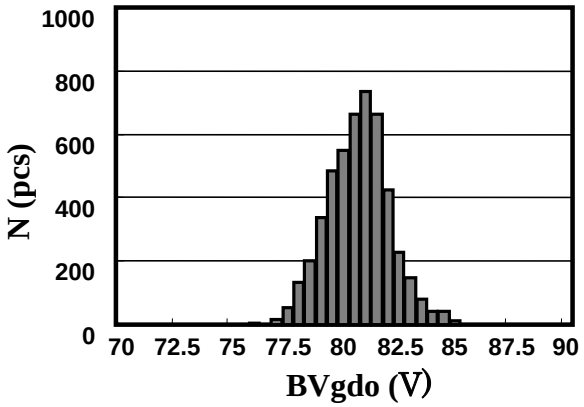


*Fig.5. (a)* The gate-to-drain breakdown voltage (BVgdo) @Igd=-0.5 mA/mm

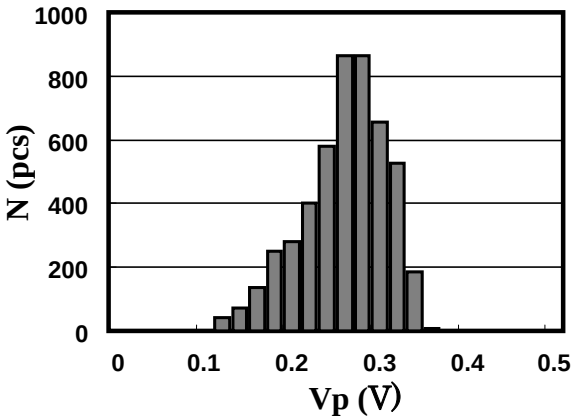


*Fig.5. (b)* pinch-off voltage (VP)

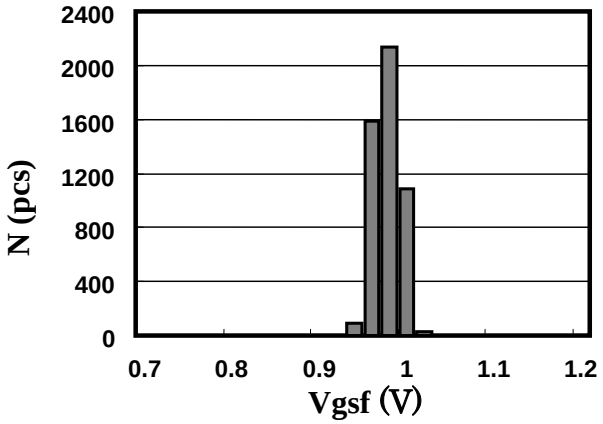


*Fig.5. (c)* The gate-to-source forward voltage (Vgsf) @ Igs=0.5 mA/mm

*Fig.5. (a) ~(c) Distribution data of on wafer process.*

The FET shows good repeatability through the mass-production wafer-lots. The average BVgdo of 80.5 V with the standard deviation of 1.4 V are obtained. Such a good repeatability enables the reduction of time and cost for the actual amplifier manufacturing.

## FET PERFORMANCE

Using this technology, 4W to 90W chips are developed and now used in volume for several FET products. As an example, the outline of the 250 W push-pull FET is explained. The FET is consisted of four pieces of the 90 mm gate width FET chips in a push-pull configuration. Figure 6 shows a photograph of the 250 W push-pull FET.

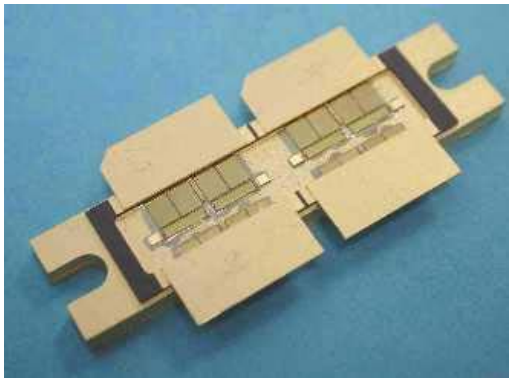

*Fig.6. Photograph of 28 V 250 W FET*

Figure 7 and 8 show the measured out-put power performance of the push-pull FET at 2.14 GHz. A saturation power of 54 dBm (250 W) and linear gain of 15.5 dB are obtained. It also exhibited a power added efficiency of 25 % at an output power of 46 dBm.

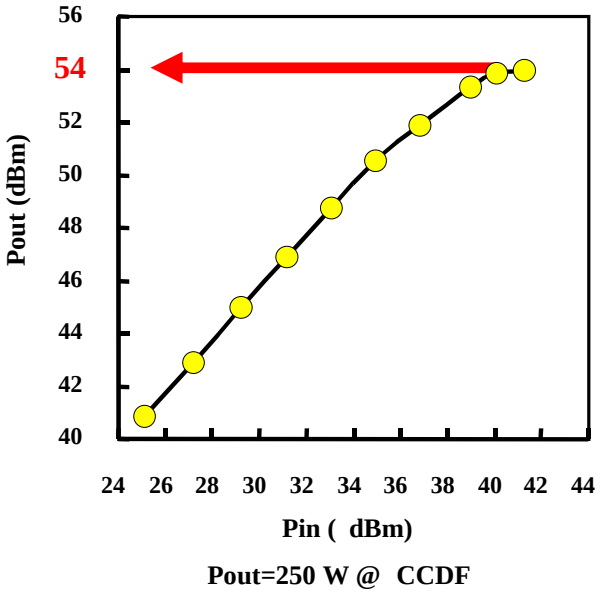


*Fig.7. Pulsed CW performance of push-pull GaAs FET at Vds=28 V and Idsq=1.5 A. Measured frequency is 2135 MHz*

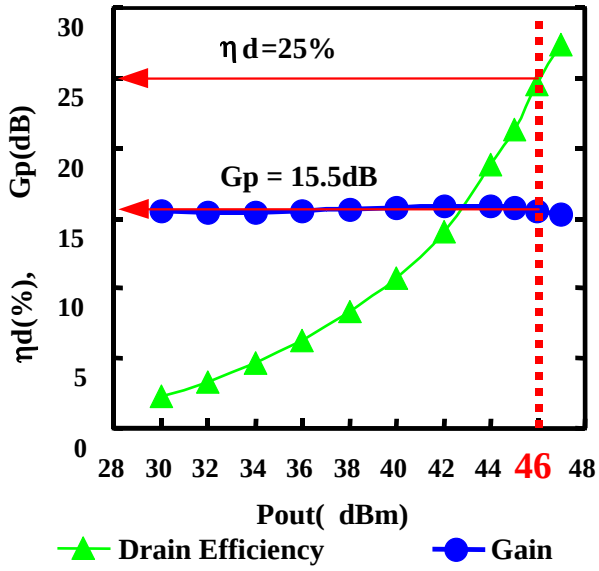


*Fig.8.One-carrier RF performance of push-pull FET. Measurement was carried out by using a non-clipping W-CDMA test signal and measured frequency of 2132.5 MHz. Bias condition is Vds=28 V, Idsq=1.5 A.*

## RELIABILITY

The devices used for infrastructure applications such as base station system are also required to present a high reliability. A high temperature operation test has performed to estimate mean time to failure (MTTF) of the device. The channel temperature (Tch) and Vds was set to 240 deg-C and 32 V, respectively. The failure criteria were defined as power reduction of more than 0.5 dB or gain reduction of more than 0.8 dB. The test was performed up to 2000 hours and no failure sample was observed. Since the activation energy (Ea) could not be determined at present, the Ea of 1.2 eV, which was obtained from our previous study for a similar type of FET, was assumed.

The estimated Arrhenius plot for MTTF is shown in Figure.9. Arrhenius' equation is defined as follows;

MTTF =A exp (Ea/kT)

Ea: Activation energy
T: Absolute temperature
k: Boltzmann constant
A: constant

The solid and dotted line indicate MTTF at Vds of 32 V and 28 V, respectively. The estimated MTTF is greater than at least 4 x $10^6$ hours at Tch of 145 deg-C.

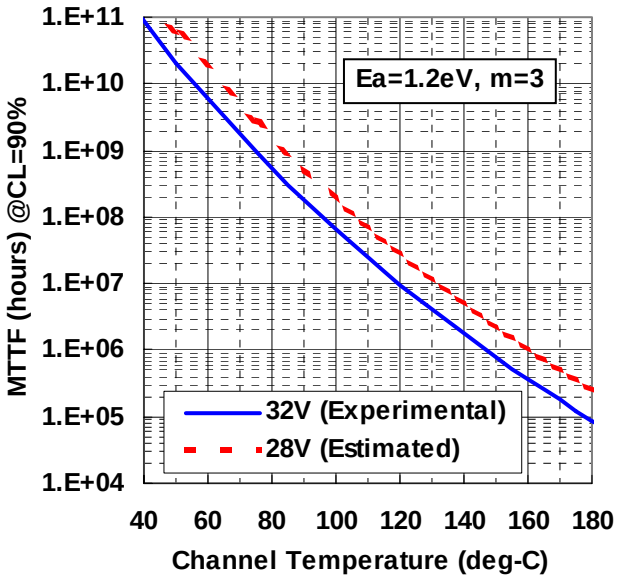


*Fig.9 Estimated MTTF versus channel temperature*

## CONCLUSION

We have developed the high breakdown voltage GaAs FET. The technology has a typical breakdown voltage of 80.5 V allowing a operation at 28 V drain voltage. By utilizing this technology, devices capable of 250 W have been successfully demonstrated. Through the process and parameter optimizations, the device also shows very good repeatability and reliability. The estimated MTTF at Tch of 145 deg-C is greater than at least 4 x $10^6$ hours. The actual production data of the standard deviation of BVgdo is 1.4 V. The developed 28 V GaAs FET technology is very attractive for high power base station amplifier applications.

## ACKNOWLEDGEMENTS

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## REFERENCES

[1] K. Ebihara, K. Inoue, H. Haematsu, F. Yamaki, H. Takahashi and J. Fukaya, "An Ultra Broad 300W GaAs Power FET for W-CDMA Base Stations", 2001 IEEE MTT-S Digest, pp. 649-652.