Stepper Based Sub-0.25μm Process for mm-Wave Applications

Matthew F. O'Keefe, James G.E. Mayock, D. Mike Brookbanks,
Jason McMonagle and John S. Atherton.

Filtronic ICS, Newton Aycliffe, County Durham, DL5 6JW. UK.
Phone + 44 1325 301111, Fax + 44 1325 306600, email matthew.okeefe@filtronic.com

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Abstract

The stepper based volume sub-0.25μm GaAs pHEMT process utilizes 5 inter-level metallizations and three dielectric layers for high frequency performance whilst maintaining the economies of scale of 150mm (6") diameter substrates. The process has recently been used to fabricate X-band and K-band MMICs, showing excellent performance and yield. The approach taken here with DUV stepper and 150mm wafer diameter will lead to a significant cost reduction for MMICs up to 30GHz.

INTRODUCTION

Significant opportunities exist for GaAs MMICs for commercial applications such as digital radios for cellular backhaul (6-40 GHz), VSAT ground terminals (27-31 GHz), automotive radar (76-77GHz), and the typical military applications such as air-borne radar and electronic warfare. Although far smaller in volume than the cellular and WLAN applications the unit sell price remains higher for these applications.

GaAs processing technology, specifically for cellular applications has benefited from significant investment in processing equipment, new FABs and increased wafer diameter leading to very high yielding, extremely low cost products. Typically, high performance millimeter wave MMICs have been based on 3" and 4" wafer diameter processes and e-beam lithography leading to high unit sell price, low yield and variable performance. Ideally, millimeter wave MMIC technology should leverage the advances that have been made in the handset arena.

Filtronic has developed a number of process technologies [1,2] that utilize modern GaAs processing techniques to provide high volume, low cost products for a range of wireless infrastructure and cellular handset applications. It has recently developed a new high performance millimeter wave power process (FD25) targeted to provide high performance and low cost based mainly on the existing high yield, proven process modules, such as deposition and etch. Uniquely, we believe, we have integrated DUV stepper technology for sub-0.25μm gate formation, with 150mm wafers to provide a state of the art millimeter wave process. This process should ideally suit the high performance commercial and military markets that are emerging.

PROCESS

The Filtronic FAB uses a series of standard modules to construct its process routes. All routes are 6" (150mm) pHEMT technology, based on an AlGaAs/InGaAs/GaAs structure, grown by MBE. The active portion of the device consists of an undoped InGaAs channel sandwiched between two silicon planar doping layers, separated from the channel by un-intentionally doped AlGaAs spacer layers. The structure has doped cap layers optimized to simultaneously achieve low on-resistance whilst maintaining high breakdown voltage. The device fabrication uses a selective ICP (Inductively Coupled Plasma) dry etch to define the recess and achieve uniform pinch-off voltage across the full area of the 150mm wafer. Dry etching of GaAs is achieved using a chlorinated gas chemistry. Selectivity is achieved by optimization of the gas chemistry.

NiAuGe ohmic contacts and TiPtAu gate, local interconnects and interlevel metallizations provide external connects. A novel deposition procedure enables thick film metallization with fine line alignment and low tolerances to be achieve over the full 150mm wafer area. A 'T' gate metal technology ensures a low gate resistance. Resistors are provided using both epitaxial layers and TaN thin films. All fabrication processes provide a zero handling environment to achieve high yields and uniform characteristics.

Silicon nitride layers provide encapsulation and capacitor dielectric. Several dielectric films are used facilitating the formation of different capacitances per unit area. These films of silicon nitride (SiNx) are deposited by means of plasma enhanced chemical vapor deposition. All deposition processes were developed to minimize the effect on the DC and RF parameters of the fabricated

components. Specifically, breakdown voltage (BV_{DS}) and maximum current (I_{MAX}) are unaffected by the deposition. Pre- and Post-deposition electrical characterization formed an integral part of the development cycle. Particular attention has been paid to these processes to achieve high reliability and environmental protection. An optional protective overcoat layer provides handling robustness.

Dry etch processing is also used for the through-substrate via. Optimization of this process required excellent across wafer uniformity, accurate end-point detection and minimal back sputtering of the front-side metallization. The etch is performed using a Unaxis VLR700 system. Maintaining a high selectivity to resist also ensures a high via yield and small feature size.

In addition to these characteristics the 0.25µm mm-wave pHEMT (FD25) process combines high-power and low-noise operation up to 50 GHz through the epitaxial and cross-section design. An extra metal interconnect layer provides three MIM capacitance densities. The "cap-on-via" and "source-on-via" process assists size compaction and offers low inductance grounds for higher frequency performance. Fine line air bridges produce minimal interconnect capacitance and improved performance. Wafers are thinned to 50µm for improved thermal and RF performance. Table 1 provides typical transistor characteristics. Figure 1 demonstrates excellent within wafer, within lot, and lot-to-lot uniformity for end of line F_T. Figure 2 demonstrates the excellent circuit appearance. Great care has been taken to ensure that end of line visual inspection can be carried out by automated tools. The use of such tools further reduces total manufacturing cost.

TABLE 1. TYPICAL TRANSISTOR CHARACTERISTICS

Symbol	Parameter	Typical	Unit
I_{MAX}	Maximum current	550	mA/mm
I_{DSS}	Drain Current	280	mA/mm
BV_{DG}	Breakdown Voltage	-16	Volts
F_T	Transition Frequency	50	GHz
G_{MAX}	Max Available Gain @ 10GHz	18	dB
V_P	Pinch-off Voltage	-1.0	Volts
I_{GS0}	Gate-source leakage	-1	µA/mm
G_{M0}	Intrinsic transconductance	500	mS/mm
R_{ON}	On Resistance	2	Ohm.mm

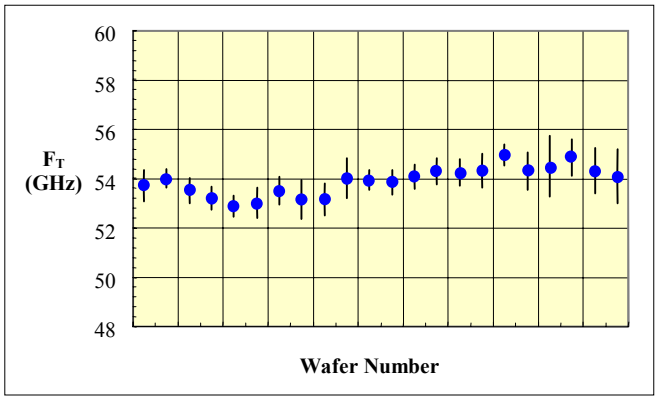

FIGURE 1. RF-PCM F_T FOR RECENT LOTS

PROCESS DESIGN KIT

A full Process Design Kit has been created for the process that supports both electrical (circuit simulation) and layout. The kit has been developed for AWR's Microwave Office design environment. It provides a full range of both active and passive components for MMIC development that are, by definition, correct by construction. Within the passive component set are a range of spiral inductors, tantalum nitride and epitaxial resistors, multilevel transmission lines and MIM capacitors. The use of three process metal layers enables the creation of capacitors with low, medium and high capacitance (200 to 1000pF/mm^2) values for optimum circuit design, by selecting the appropriate combinations of dielectric layers within the capacitor. As the process has been developed to utilize 50µm thick substrates this allows the generation of through GaAs vias with diameters from 30µm, which can also be extended into elongated slots. Capacitors on vias are also available for improved circuit designs. Models for these capacitors have been derived from S-parameter measurements and validated by EM simulations.

The active components utilize the through GaAs vias in the elongated (slot) format to place a local via under the source regions of the FET for minimum source inductance and improve the scalability of the devices to larger total gate periphery. Scaleable models for these devices are available within the Design Kit. For small signal electrical simulation model fits to measured S and Noise parameters are used, whereas for large signal simulation either TOM3 or Parker-Skellern models are provided.

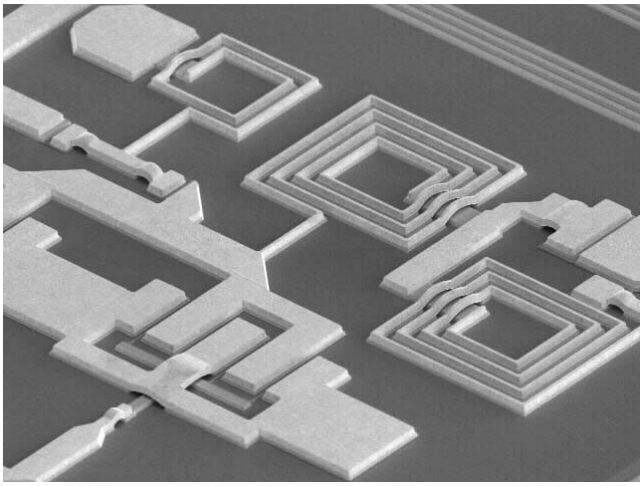

FIGURE 2. IMAGE OF CIRCUIT FABRICATED USING FD25

PRODUCT DESIGN

The high breakdown and excellent high frequency performance of the FD25 process makes it attractive for a number of applications up to millimeter-wave frequencies. Stepper based technology offers the potential for high yields, which is particularly attractive for some of the emerging higher volume microwave and millimeter-wave markets. One such example is high power X-band amplifiers for airborne radar applications, where there is a continuous requirement to reduce the weight and cost of TR-modules and still obtain high PAEs and output powers. Adequate performance can be realized using 0.5µm technology, but significantly higher PAEs and gains can be achieved using the FD25 process. The enhanced component technology on the FD25 process, such as the inclusion of slot vias and cap-on-vias, means novel circuit configurations, reduced circuit size and enhanced performance can be achieved.

A set of two-stage MMIC amplifiers was designed to operate over the 7-11GHz range. A set of load pull measurements was used during the design stage to find the optimum load impedance for power density, and trade-offs for PAE. Power densities of greater than 0.6W/mm and PAEs of better than 50% were obtained for a 10x120 micron device. Further improvements to the PAE could be obtained by harmonic tuning at both the source and load during these measurements.

It was decided to use an output periphery that consisted of eight cells of 10x120 microns. Careful consideration was taken over the unit finger width and the gate-gate spacing in order to minimize thermal effects, and maximize the gain without resorting to an excessively large y-dimension of the chip. The driver device consisted of two 10x100 micron devices. It is important for the driver device to be significantly large, such that output device saturates first, but also not excessively large such that the extra DC power impacts significantly on the PAE of the MMIC amplifier. The pHEMT cells in both the driver and output circuits included stabilization networks. It is critical to stabilize the cells at out of band frequencies, without losing excessive amounts of gain in band.

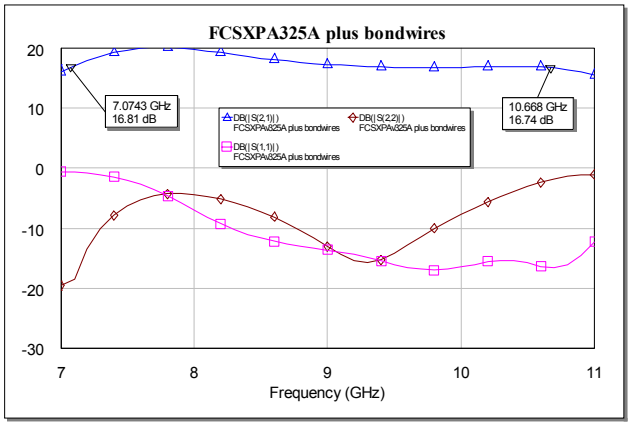

FIGURE 3. SMALL-SIGNAL RESULTS FROM THE X-BAND HIGH POWER AMPLIFIER

On-wafer small-signal measurements were carried out on the MMIC amplifiers. Approximately 17dB of gain was achieved between 7-11GHz, with excellent input return losses measured between 8-11GHz. The output matching circuit is designed so that maximum power is extracted from the device, which results in a relatively poor output return loss. In TR modules two MMIC amplifiers are balanced externally which gives good matches at both the input and output. Figure 3 shows a plot of the measured parameters recorded at a low VDS (3V). Presently the MMIC amplifiers are being characterized under pulsed conditions.

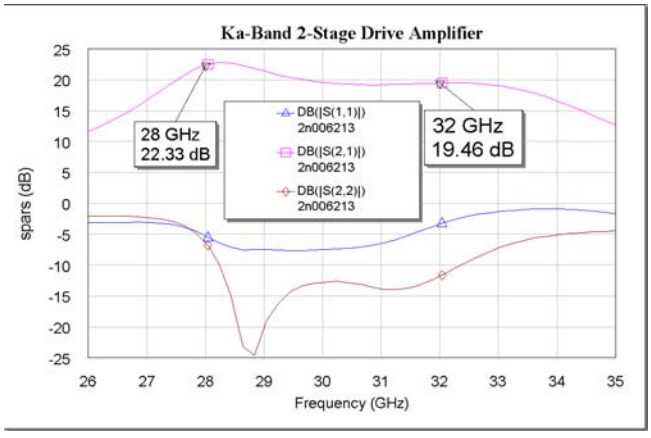

FIGURE 4. SMALL-SIGNAL RESULTS FROM THE 30GHZ MPA

A set of two stage amplifiers has been designed to operate in the 30GHz range of VSAT applications. These amplifiers were designed to deliver approximately 20dB of gain and 23dBm of output power. The design procedure followed similar steps to those described for the two-stage X-band power amplifiers. Figure 4 shows a plot of measured S-parameters for one of the driver amplifiers. Excellent performance was obtained with close to 20dB gain at 30GHz. The saturated output power was measured to be 22dBm. In both cases, the measured performance agrees well with simulated data.

CONCLUSIONS

This paper has outlined the development of a high performance 0.25µm process on 150mm wafers using a DUV step-per for the gate formation. The process builds very successfully of the 0.5µm technologies developed at Filtronic and shows excellent performance and yield. Initial product development using the process is proceeding well and initial results on an X-band HPA MMIC and 30GHz MMIC amplifier demonstrate the success of the approach. This technology is ideally suited to high performance, low cost mm-wave applications.

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ACRONYMS

FET:	Field Effect Transistor
pHEMT:	pseudomorphic High Electron Mobility Transistor
MMIC:	Microwave Monolithic Integrated Circuit
DUV:	Deep Ultra-Violet
HPA:	High Power Amplifier
MPA:	Medium Power Amplifier
VSAT:	Very Small Aperture Terminal
WLAN:	Wireless Local Area Network
FAB:	Fabrication Facility
MBE:	Molecular Beam Epitaxy
PAE:	Power Added Efficiency
TR:	Transmit Receive
EM:	Electro-Magnetic
TOM3:	Triquint's Own Model -Version 3