Outstanding Issues in Compound Semiconductor Reliability

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Abstract

Can we proclaim that Compound Semiconductors are reliable? This discussion is meant to look back at progress in reliability evaluations over the last two decades, identify a few items that have been learned, and select what challenges remain. While addressing various issues, it is the accumulation of data and information which forms the basis of an assessment of reliability. In the end, reliability is simply an insightful perception of stability and maturity, based upon experience.

INTRODUCTION

Compound Semiconductors (CSs) have been around since the beginning of solid state technology, but the commercialization and "catch up" phase started in earnest just about 20 years ago. Although it has a certain allure, new technology unfortunately carries a suspicion of reliability risk. This discussion will address the question: How have CSs done with reliability over the past 20 years? After this brief review, we will turn to: What's left to be done in compound semiconductor (CS) reliability? To conclude the discussion, we will set a goal and an approach to use going forward to address the-best-of-the-worst in terms of those "outstanding issues."

The intent of this discussion is to provide information on:

1) Identification of the reliability issues,
2) coming to grips with the issues, and
3) offering a roadmap to address the issues.

A BRIEF HISTORY OF SEMICONDUCTOR RELIABILITY

In order to discuss reliability of CSs, let's start by looking at reported lifetimes of circuits for the past 20 years. Figure 1 was compiled from summarizing reported lifetimes at the ROCS Workshop since 1985 [1]. Note these extrapolations are normally for lifetimes of devices operating between 125ºC and 150ºC. To judge these CS results against silicon's reliability progress, let's go back 25 years, and break-up the time period into five *eras* of improvement. [2]

Prior to 1985, reliability improvement on silicon devices had already begun – and those efforts had already passed through two eras. In the first era of silicon reliability improvement, from 1975 to 1980, the **Introduction of "New" VLSI Materials** was at the forefront. Everyone was learning about material properties of Si, Al, and SiO_2 and their various interactions.

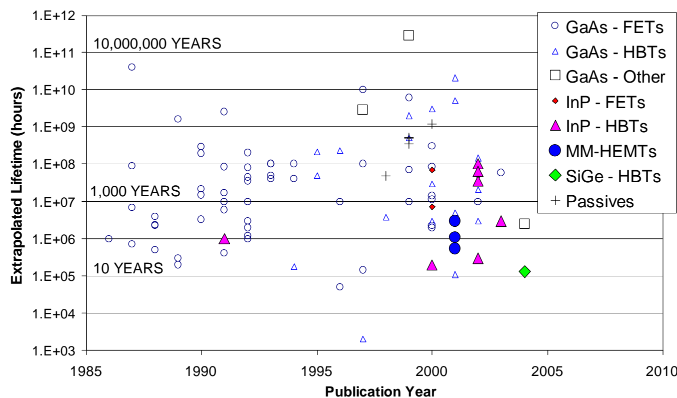

FIGURE 1. REPORTED OPERATING LIFETIMES FOR VARIOUS COMPOUND SEMICONDUCTORS OVER THE 19 YEAR HISTORY OF THE ROCS WORKSHOP[1]

In the second era, from 1980 to 1985, the **Major Reliability Problems** for silicon technologies were identified: mobile ions, electromigration, stress migration, Time-Dependent-Dielectric-Breakdown (TDDB), cracked die, broken bond wires, purple plague, and soft errors. The re-emergence of compound semiconductors was just beginning – generally with discrete devices, and then the integration of MMICs started.

In the third era, from 1985 to 1990, **Reliability Physics** was the focus for the silicon folks. They had developed degradation models (by characterizing failure distributions) for all the previously identified mechanisms. Acceleration factors were derived for the special environmental stresses of temperature cycling and corrosion. These were the showcase years for ESD studies on silicon. This was also the time that compound semiconductor circuits were introduced. From Fig.1, you can see that all the emphasis was on FET style devices during these years, primarily MESFETs. CS devices were scarce, so sample sizes were small, and the CS folks immediately took up the reliability physics methodologies established by the silicon folks.

In the fourth era, from 1990 to 1995, the silicon folks adopted a new phrase; **Building-In Reliability**. This was a period of reliability engineering, with emphasis on process control, in-line screening, and wafer level reliability. The CS folks were sidetracked with the commercialization of their technology, and the carving of a small niche in the semiconductor market. Almost all of the CS work was with FET devices, but HBT reliability work was started in the later part of this period The focus shifted from implanted devices to epitaxial circuits, so this meant even more new CS materials without the first-era and second-era reliability experience.

In the fifth era, from 1995 to 2000, the silicon folks were completing their 20-year cycle (a "generation") by merging the metrics of reliability and quality with focus on a **Major Defect-Reduction Effort**. This was characterized by statistical quality control, various six sigma programs, and a relentless search for "outliers" of measured distributions. This was the "happiest" period for CSs, as most companies were riding a huge volume increase. CS reliability emphasis was back at the second era of the silicon cycle – looking at "new" mechanisms which became more apparent with the explosion in volume shipments and the increases in sample sizes for reliability aging. You can see from Fig.1 that there was interest in passive devices, particularly capacitors, as the CS folks learned about TDDB.

From 2000 to 2005, the silicon folks have been restarting their cycle by reverting back to the first era, with the **Introduction of New ULSI Materials**. Work is on new copper metallizations, low-K interlayer dielectrics, and high-K gate dielectrics, new metal gate materials and getting features smaller than 100nm. CS reliability emphasis is also on new material – new semiconductors. Fig.1 indicates InP, metamorphic layers, and even GaN results are starting to show up on the CS reliability radar.

During this full cycle review of silicon reliability efforts and the definition of the five eras, [2] there are some interesting parallels in the CS data. While some of the techniques of the silicon cycle have been utilized during the CS development, most of the eras have not been duplicated. Elements of eras 1-3 have been investigated, but some holes still remain in the basic material properties of the CSs and the noble metallizations used. Moore's Law has not driven developments for CS interconnects or dielectrics. Instead of shrinking features appreciably, CSs tend to squeeze performance out of epitaxial enhancements and blending of additional "new" materials into the semiconductor. The eras of "building-in reliability," and "major defect reduction effort," have barely been touched by CS manufacturers. Even though the compound materials are constantly changing, a glance at Fig.1 indicates there is no significant lifetime difference from materials or from FET and bipolar technologies. In fact, there is no significant change in the overall reliability during the past 20 years! (This same complaint is also made by the silicon reliability folks) [2]

UNDERSTANDING MECHANISMS

From the first, second, and third eras of silicon reliability, everyone has learned the methodology of determining lifetimes and failure rates. The three keys to measuring and predicting reliability are:

1) knowledge of the root cause failure mechanisms,
2) measurement of degradation distributions, and
3) characterization of acceleration factors.

Obviously, the CS folks used all of the prior knowledge available from the first and second silicon reliability eras, but the failure mechanisms are not necessarily the same. There are a multitude of failure mechanisms for compound semiconductors, and recognizing that there is more than one is an "outstanding issue." Here are a few of the significant CS mechanisms in a relative chronological order of discovery and publication:

Sinking Gates. This diffusion mechanism is thermally driven. It is one of the oldest reported for FET-style compound semiconductors. The diffusion has been substantiated with physical evidence for both MESFETs [3] and pHEMTs [4]. Because the sinking mechanism is so easy to accelerate with temperature, sinking gates are often identified as *the* cause of FET wearout. Even though some refractory gate metals have been aged and reported, titanium is still a common material for FET gates, and Ti diffusion with GaAs is exponentially accelerated with increasing temperatures. In reliability terminology, sinking gates have a very high activation energy. Even though the activation energy has been empirically measured at 2.56eV [5], it is not unexpected based upon diffusion of other transition metals in GaAs; Mn = 2.49eV, Au = 2.64eV, and Ag = 2.27eV. So if we were to make an estimate of the activation energy for Ti diffusion in GaAs from the Ballistic Model, it wouldn't be a stretch to 2.56eV since the enthalpy of formation of a gallium vacancy has been estimated by Van Vechten to be 2.31eV.[6] This mechanism is quite unique to the Schottky contact FETs, and nothing like the mechanism found and addressed in the MOS-type world because the acceleration is an order of magnitude higher.

Gate Lag. "Lag" is a common affliction of FETs. This phenomenon is thought to be a result of traps on the GaAs channel surface beside the gate. But is gate lag a reliability failure mechanism, or merely an ugly property of trap-filled compound semiconductor substrates? Investigations into the aging of traps have indicated no particular degradation over time. [7]

Hot Electrons. Borrowed from problems suffered by silicon gate dielectrics, this is a charging effect, sometimes called "power-slump." This is indeed an interesting mechanism, since it is exacerbated by high electric fields and by low temperatures – at least for oxide dielectrics. The degradation is caused by impact ionization at the gate edge, which injects hot carriers into the interface between the semiconductor and insulator. These carriers effectively expand the surface depletion layer and reduce Idss and gm without much of a change to the threshold voltage. [8]

Mechanical Stress. Compound semiconductors are piezoelectric. [9] Local mechanical stresses will cause changes in fields and characteristics of active devices. Yet when hydrogen contamination was found to cause threshold shift degradation in CS FET devices (in 1989), this piezoelectric degradation was passed-over for a more *sexy* theory "…conversion of gaseous hydrogen into atomic hydrogen in the Pt layer of the gate metallization, and the subsequent doping compensation and carrier removal from the active channel as the atomic hydrogen diffuses into the channel."[10] It has taken more than 10 years to bust the original beautiful theory with the simple ugly fact that reduction of the gate metals (particularly titanium) in hydrogen produces a compressive stress that causes a piezoelectric polarization charge and results in the threshold shift. [11] This is another mechanism foreign to the silicon guys.

Electromigration. This is an example of a failure mechanism born from silicon experiences. Aluminum metallization is particularly susceptible to electromigration because of its relatively high resistivity. Aluminum also has a grain structure that makes it vulnerable to failure. Most CSs use gold instead of aluminum. The electromigration mechanism can be induced in gold under very high current densities, but electromigration has been largely disregarded for compound semiconductor interconnects at current densities below 500,000A/cm^2.

Current density does seem to have an accelerating effect on HBTs. [12] But there are two diverse theories as to the cause. From the GaAs blend folks, the latest account for increasing base current is the "tunneling-recombination conduction mechanism." [13] From the SiGe folks, "change in ß is attributed to electromigration induced *pressure* on the emitter contact." [14] There continues to be significant experimentation with thermal acceleration aging and both theories discuss results within the acceleration context of activation energy instead of current density. It is clearly an "outstanding issue" that current density is known to be the primary stress to accelerate degradation in HBT devices, and most aging is still accelerated by temperature? It also seems to be an issue that at least two different mechanisms are claimed. Could both arguments be correct?

Corrosion. Moisture ingression has only recently been considered as an issue for compound semiconductors.[15] Although gold and nitride are thought to be relatively inert; many of the CS contact materials are susceptible to moisture as are some of the semiconductor materials. In the past couple of years, humidity testing has come to the forefront. Once again, the CS mechanisms were found to be substantially different from those characterized and modeled originally with silicon material families.[16] Nevertheless, significant lifetime improvements based upon various surface treatments are still being made for CS FETs.[17] It is interesting, even within this short review of selected failure mechanisms, that a 2004 look at the root cause of moisture degradation takes us back to the early piezoelectric/mechanical stress mechanism.

FAILURE DISTRIBUTIONS & STATISTICS

Living with Distributions. To characterize reliability, folks need to know about degradation distributions. Significant degradation is needed during aging and the ability to separate fallout by each mechanism is often the issue. This can be especially difficult in a complex IC where multiple mechanisms are all degrading at various rates, in opposite directions, and under the influence of multiple forms of acceleration. Reliability engineers tend to differentiate these problems with complicated statistical formulas and probability estimates in order to evaluate all the complexities. While this approach may seem to bring out unbiased and objective interpretations of the results, it often is where the non-reliability person gets lost. Unfortunately, even the reliability engineer often looses sight of what might be most important for customers and the distributions behind the data (Fig.2).

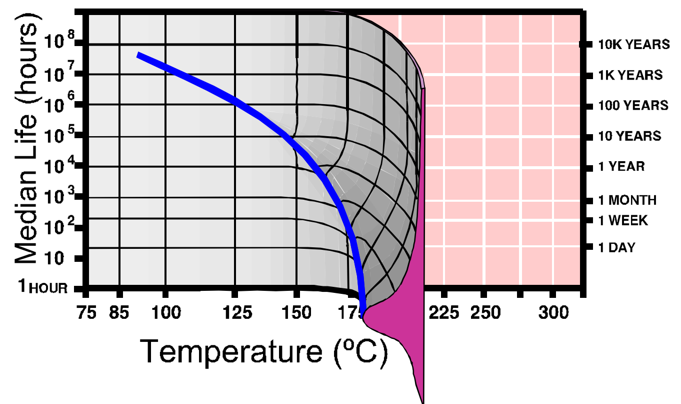

FIGURE 2. REPRESENTATION OF DISTRIBUTION DATA THAT UNDERLIES SIMPLE LINES SHOWING MEDIAN LIFE DEPENDENCE ON TEMPERATURE.[17]

Even though reliability engineers and statisticians will enjoy analyses of distributions using Normal, Lognormal, Weibull, Poison, Maximum Likelihood, or some other techniques, they all tend to show nearly identical (albeit astronomical) results after the acceleration factors are considered. In other words, small differences between distributions aren't significant when each method projects median lifetimes that are 180 orders of magnitude larger than the known age of the universe! [18]

Squeezing the Curve. Once the distribution is known, how do we make use of it? One of the most *outstanding* issues in CS reliability is interpretation of results. For example, reliability engineers speak in terms of "median" lifetimes – when half of the population will fail. The issue is that customers want to know when the *first* part will degrade. Typically, this question begins another mathematical diversion into confidence levels and probabilities – more gobbledygook for those not familiar with reliability. A not-so-obvious answer could be to reduce the dispersion of the distribution, so that the time to the first failure and time to 50% failure are closer together. Another idea would be to dump references to median time, and report data for the first failure, such as a t_{ppm} (time to first part per million fail) instead of t_{50} (time to 50% failure.) Once the distribution shifts from the "middle" to the "front edge," any separations between quality and reliability start to come together – as was signaled in the silicon generation; this is an indicator of the fourth era.

USING THE *RIGHT* ACCELERATION

If we are to make predictions about reliability, we must be able to accelerate the failure mechanisms without generating new issues or masking mechanisms that may exist under reduced stress. Thermal acceleration is easy, but that doesn't make it the right thing to do. Understanding of mechanisms and degradation distributions can help us to look where acceleration might be less understood. To help, we need to talk more with our customers. Their use of the devices can give use clues as to what types of acceleration are more applicable. For example, thermal excursions, voltage, current density, and humidity might be preferable to high temperature acceleration. In other words, almost every part gets attached by a solder reflow (an extreme thermal excursion). Hopefully, the devices will all turn on (experience voltage fields and current flow). And eventually, parts under normal use are likely to be exposed to an everyday environment (humidity).

We can investigate the applicability of various stresses by talking with customers, or by use of an effectiveness chart. Remember, reliability folks need some kind of degradation to measure and predict metrics, so effectiveness means: how well do aging tests cause failure? Since we've already admitted that changes in reliability are meager, this type of graph is useful to guide our improvement efforts.

OVERCOMING DENIAL

How does one define an *issue*? For any situation, a good answer is: ask your customer. For a reliability issue, just look at what causes your customers to return devices. Figure 3 shows the causes of device returns for five years. Notice that **none** of the problems that our customers report match with the six mechanisms previously mentioned in the historical recap! This shouldn't be a surprise because most lifetime projections from Fig.1 don't predict any wearout for hundreds (even thousands) of years.

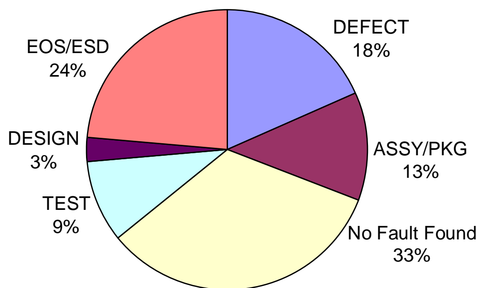

FIGURE 3. RESULTS OF ROOT CAUSE FAILURE ANALYSIS OF FIELD RETURNS SINCE 1999. TRIQUINT SEMICONDUCTOR DATA.

What can be more of an issue than a customer failure? If the stresses don't simulate what a customer does to the device, and the failures aren't the same type that our customers report, then how can *the good old approach* predict reliability? Following is a discussion on the top two actual causes of failures from Fig.3.

ESD. From Figure 3, ElectroStatic Discharge is the leading cause of problems reported by customers. This has been true as long as we have measured the causes. However, the compound semiconductor folks have tried to explain away this weakness as a technology difference or an application education problem. ESD is definitely an "outstanding issue."

Defects. The second leading cause of customer problems is eventually going to be defects. However, this is not as clear an issue as ESD. Defects seem to rise up in the Pareto chart as all the other causes get solved and processes mature. Assembly and packaging or testing issues will sometimes outweigh defect issues in development phases. But if improvement is made, defects will eventually come up - remember the fifth era of silicon reliability improvement? Era five was 5 years of a "major defect reduction effort." So, acknowledgement of defects as a CS issue is a positive sign that CSs are indeed following the path of maturation demonstrated by silicon reliability experiences.

The most commonly reported CS defects are found in capacitors. Several compound semiconductor manufacturers have reported studies on capacitors. [19,20,21,22] The mechanisms, distributions, and acceleration factors are understood and similar to what has been found on silicon devices – particularly for the focused improvements on ever thinner gate dielectrics.

Other defects involving interconnect integrity and metal-to-metal leakages are newer issues for compound semiconductors. The distributions are familiar, but the mechanisms and acceleration factors appear to be specific to the technologies involved. Understanding these differences is likely to be one of our next challenges. [23]

KNOWING WHAT WE KNOW

With few exceptions, the reliability investigations on GaAs circuits over the past two decades have evolved to rely on thermally accelerated wearout failure mechanisms. See Figure 4. Regardless of the measured lifetimes, there have been no circuit wearout failures reported during use of the circuits. Instead, customers do report measurable defect rates and early life failures that often match-up with yield fallout failure mechanisms, and occasionally a maverick lot. In this discussion the various mechanisms have been summarized, while focusing on issues that correspond to many of the early life failures.

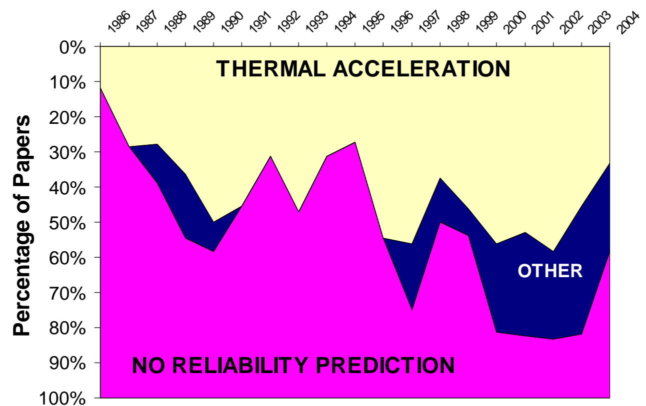

FIGURE 4. TYPE OF ACCELERATION REPORTED AT THE RELIABILITY OF COMPOUND SEMICONDUCTOR WORKSHOP (ENTIRE WORKSHOP HISTORY).

STRATEGY TO BEAT SILICON

So now that some of the "outstanding" issues are exposed, what should be done about them? We propose a new goal for CSs: beat silicon! For 20 years, we've touted the technology differences as a defense for the compound semiconductor niche; why not use the reliability differences to our advantage as well? Because of the unique mechanisms and absence of the silicon problems, CSs have an opportunity to use diversity to build a better "burn-in" and optimize the Bathtub Curve.

In spite of our silicon rival's size, it is not so wild a notion that the CS technologies could actually prevail in terms of a reliability comparison. Even with a full set of six eras under their belt, the silicon folks have a number of "outstanding issues" of their own yet to solve. The relentless pursuit of Moore's Law has contributed to a new cycle of reliability challenges for the silicon technologies. Materials for mainstream silicon are new once more, and the engineers began the second generation of reliability improvement at the turn of the century, with most of the first era completed (again). 2005 is the cross-over year to begin characterization of new mechanisms for the silicon folks as they enter their second era.

BEING INNOVATIVE

Armed with the issues and the goal, there are a few obvious tactics available to compound semiconductor companies. Some tactics can be turned-around upon the silicon folks, and some are unique. As the overall reliability improves, degradation becomes elusive. If the CS folks intend to build experience that is familiar to the customers, we should proceed with tactics of building-in reliability and efforts to reduce defects. An illustration might be a more visible use of yield-to-reliability correlations as an example to predict failure rates. If yield fallout also disappears, we can use new tricks such as *physical amplification* of defects in order to extend our predictive capability.[23] Other recent CS breakthroughs with innovative tests such as "bubble tests,"[24] and power cycling [25] are the kind of tactics that can put CSs ahead of our larger solid state relatives.

SUMMARY

If CS reliability is to be measured by the silicon yardstick, then there are two areas of focus with several important tasks ahead:

1. Formalize the CS knowledge from the initial three reliability eras.

   Identify, define, and characterize the failure mechanisms for all CS materials in use. It's also important to match up the mechanisms with appropriate distributions and acceleration factors. That means high temperature stress shouldn't be utilized when current density matters! The rigors of reliability physics are necessary for all mechanisms, not just when high temperature acceleration is employed.

2. Embrace the tactics of era 4 and 5 quickly and openly.

   Era 4 means more effort on building-in reliability. CS folks need to showcase progress on process control and the relentless search for mavericks, rouge lots, and outliers. There must be continued development of fast, on wafer, test structures to speed reliability advancements and new material implementations. It will be important to apply knowledge of telltale failure signatures and customer returns with the use of in-line screening. Biasing methods of over-voltage, over-current, over-power are expected while quiescent and leakage current monitoring show promise. Perhaps hot or cold chuck probing will be needed as well.

   The defect reduction efforts of era 5 offer new territory to apply innovative tactics such as defect amplification, use of new environments, and/or pioneering accelerations to put CSs ahead of silicon.

CONCLUSION

Customers are familiar with the silicon generation of reliability progress accomplished by the past 25 years of continuous improvement. Customers also have experience with problems of new technology, and a perception that compound semiconductor reliability may be lagging the main stream.

The final success at resolving "outstanding issues" will be showing customers that compound semiconductors actually have a desired level of experience, maturity, and stability in terms of reliability.

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ACRONYM LIST

CSs: Compound Semiconductors CS: Compound Semiconductor
ROCS: Reliability Of Compound Semiconductors Workshop.
Formerly known as the GaAs REL Workshop from 1985-2003.
IRPS: International Reliability Physics Symposium
TDDB: Time Dependent Dielectric Breakdown
MMIC: Monolithic Microwave Integrated Circuit
BIR: Building-In Reliability or Built-In Reliability
WLR: Wafer Level Reliability
SPC: Statistical Process Conrol
HBT: Heterojunction Bipolar Transistor