Manufacturing Engineered wafers for GaN RF power applications

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Abstract

In this paper we present recent material advances developed on the MBE growth of GaN on high resistivity low cost Si Substrates (up to 4 Inches). The recent results achieved by the GaN HEMT on Silicon in term of RF performances and reliability, bring Picogiga material as the state of the art. In combination with our MBE technology, engineered substrates using Smart Cut™ technology have been developed to improve the thermal dissipation and RF performances. The Smart Cut™ approach allows the transfer a thin layer of one material onto a base substrate of another material to combine their properties in order to overcome specific limitations for advanced applications.

INTRODUCTION:

In the next generation communication system, digital rate transmissions are going to be extensively employed. Covering a wide frequency range from S-Band to Ku-band, either commercial or military defense applications develop architectures more and more sophisticated to satisfy the communications systems requirements. Consequently, the RF transmitter-receiver module, and particularly the Power amplifier, has to match new requirements in term of power, efficiency, bias conditions and so on… The table 1 lists different applications like 3G, WLAN or WiMax and radar applications, for which the Power Amplifier specifications require to get both high power and high efficiency.

Applications	S-Band	X-Band	Broadband	
Frequency (GHz)	2-4	6-8	2-6	6-18
Power (W)	50	20	20	15
PAE (%)	50	>40	>30	>30

Table 1: Power and PAE required for different type of applications

Such stringent performances require the development of new device process technologies using new materials. The GaN material opinion has changed from a promising candidate to a serious competitor to develop high power amplifiers. The RF performances achieved by several different partners listed in Table 2, proves that the GaN on Silicon outperforms all the other material technology developed on GaAs or Silicon.

Table 2: Recent performances achieved on Picogiga materials

Partner	Michigan Univ. *	TIGER **	Triquint ***
Substrate	Si (111)	Si (111)	Si (111)
Lg (um)	1	0.3	0.3
IDSS (mA/mm)	1.2	0.925	0.85
gm (mS/mm)	340	250	220
Ft (GHz)	25	30	24
Fmax (GHz)	43	72	47
Power Density (W/mm)	1.5 @ 5GHz	1.9 @10 GHz	7 @ 10 GHz (1)
		2.6 after passivation	3.9 @ 10 GHz (2)
PAE @ Pout max	49	18	39 (1)
			52 (2)
Bias	15-30	15-30	20-40
BVds	>50V	>120V	70V

By increasing the power density by a factor 10 to 30, the device size will be shrunk, and then will ease the PA module's integration into the final communication system.
A good thermal dissipation is required to keep good performances. Picogiga has developed a growth technique using Silicon substrates. The silicon substrate is a good compromise between thermal budget management and size's and quantity's availability. Compared to the SiC substrates alternative, the Si (111) solution is a low cost technology using substrates up to 4 inches.

MBE PROCESS:

The growth process is based on the Gas Source Molecular Beam Epitaxy (MBE) with ammonia as a nitrogen source. This process is very reliable. Indeed no failure on specific cell or heaters has been observed for the past 5 years.
To maintain its leadership in the low cost approach of GaN growth on Si(111), Picogiga Int. has created different standards of Epi, named SP1 (Super Piezo 1), SP2 and SP3 in order to propose a wide choice of Epi-structures for its customers.
The standard are differentiated by the mobility and sheet carrier density results. By changing the interface between the channel and the barrier, Picogiga Int. has the capability to adjust the value of the mobility from 1500 cm^2/Vs for SP1 up to 2100 cm^2/Vs for SP3. As shown in the figure 1, these results remain very constant against the Al content.

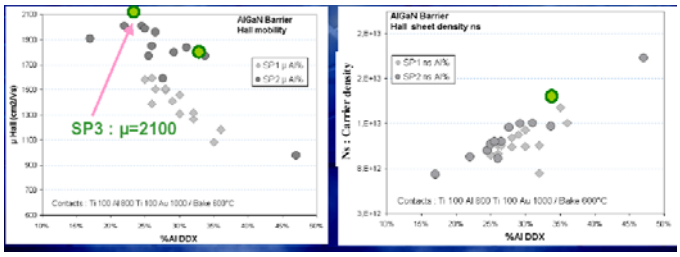

Figure 1: Electrical performances of SP1, SP2 and SP3 versus Al content.

As presented in the figure 2, the morphology doesn't change up to a high Al content of 50%. With a typical RMS roughness of 3-5 nm, the surface characteristics of the wafers are very flat and the threading dislocation is measured in the range of 10^9 cm^{-2}.

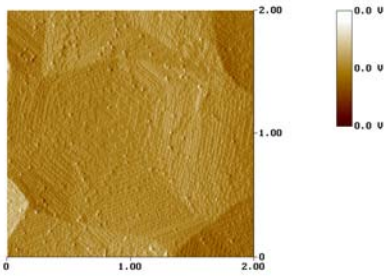

Figure 2: AFM picture of a SP3 with 39% of Al.

Based on the customers needs, the thickness of the GaN template can be adjusted from 0.5 up to 3 um is with no crack. The typical resistivity measured is above 10^6 ohm.cm.

In order to improve the template isolation, we have developed a Pseudomorphic Epi-structure. In this Epi , the GaN channel is between 2 layers of AlGaN. On both sides top and bottom, the Aluminum can be adjusted at different content without changing the electrical and surface properties.

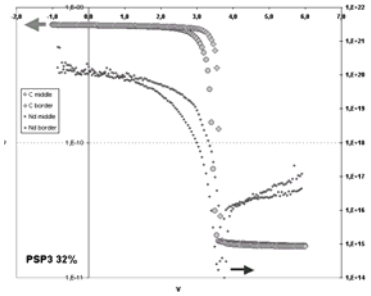

Figure 3: C-V plots of a PSP structure at 32% of Al

The figure 3 shows the CV and carrier density plots. The Pseudomorphic structure allowed a decreased of the residual carrier density by a factor of 10, preserving the HEMT electrical properties.

ENGINEERED WAFERS:

To improve the system performances, the current technologies can offer such objectives by using very sophisticated circuitries. This solution will increase the device density per circuit, the chip's size and the consumption. An alternative is to develop technologies based on new material, new devices processes and innovative techniques. The Smart Cut™ technique, well known and already established as a reference process in advanced silicon technologies (Unibond® SOI (Silicon On Insulator), emerged as the best idea to realize composite substrates to support our engineering development. Indeed the Smart Cut™ approach allows to transfer a thin layer of one material onto a base substrate made of another material, hence allowing independent optimisation of front and backside for further use of the substrate. New innovative concepts become possible for GaN epitaxy dedicated to power RF applications introducing engineered substrates composed of a thin film of Si (111) transferred on poly-crystalline SiC substrates. These composite substrates give an answer to the high power density issue improving the thermal management imposed by the high-dissipated power. As a solution for Power applications, SiOpSiC substrates (thin film of Si transferred on pSiC substrate) are a promising alternative to expensive high quality SiC single crystal substrates.

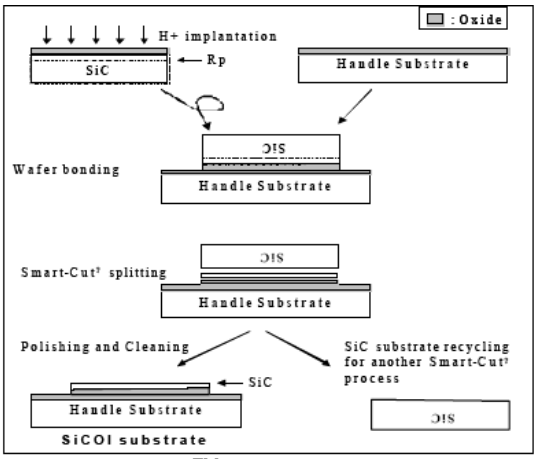

Figure 4: Smart Cut™ process flow schematic

GAN: TECHNICAL APPROACH:

Growing a material on a different material substrate generates naturally constraints at the interface. The nucleation layer is inserted in order to isolate the active layer from these dislocations. A homo-wafer epitaxy is considered to be the best solution to decrease drastically the dislocation. The smart-cut process allows to bond a thin layer of GaN on a Silicon substrate. Consequently this technique minimizes the dislocation level.

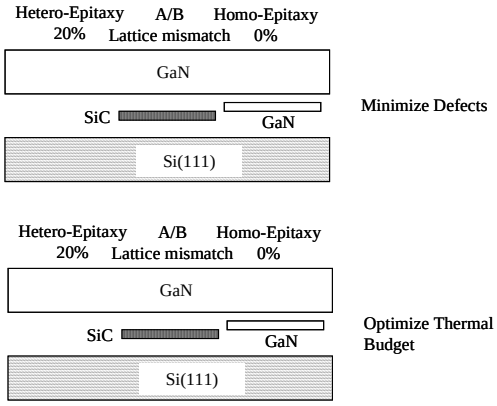

Figure 5: Materials improvements

As well known, the SiC has an excellent thermal property compared to the silicon. To make device, a high SiC quality is requiredbut it remains very expensive. An alternative is to use a poly-SiC substrate and bond it with a thin layer of Silicon or SiC to isolate the active layer from the leaky substrate.
The Smart Cut™ process allows the optimization the thermal budget without penalizing the electrical properties of the active layer.
The figure 6 shows the GaN junction temperature for several engineered wafers and at different power densities. These results demonstrate that Smart Cut™ process is suitable to develop advanced materials having thermal performances the high quality SiC.

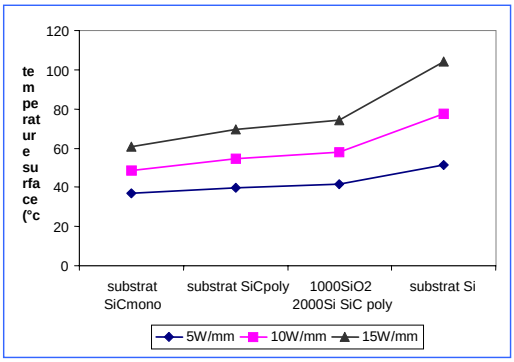

Figure 6: GaN junction temperature for different engineered wafers and power densities

MBE TECHNOLOGY READY FOR MANUFACTURING:

To compete in this battle of the new technologies, the cost has to be competitive compared to the current process. Based on the 4 inches silicon substrate, our process is definitely a low cost solution. And moving this process technology to high volume will beat any other technology developed on high quality SiC material.
Since our GaN development has started, the campaigns last longer from 2 to 6 months and the number of wafers per campaign has augmented from 40 up to 400. By growing Epi with a 4 inches multi-wafers MBE reactor, this productivity will increase by a factor 4. Once the Epi-structures fixed for production, less calibration steps will be necessary and an improvement by 30% of productivity is estimated.
After several campaigns, this process growth has demonstrated an excellent reliability and reproducibility for a wafer diameter size ranging from 2 to 4 inches. A major concern has been to preserve the structural and surface quality meanwhile increasing the length of the campaign. By improving the growth process we haven't noticed any degradation of the surface defects density or the Epi-structure through the campaign. (figure 7).

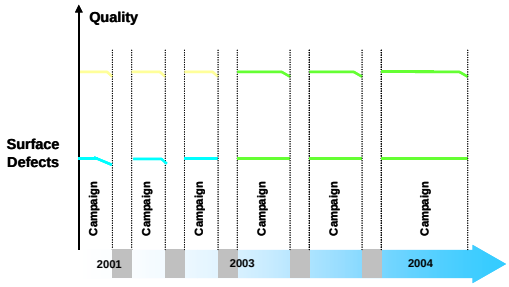

Figure 7: Improvements of the material quality and the campaign length starting from 2001 till now.

We confirm that GaN MBE epitaxy is as reliable as the GaAs one. These results guaranty us that process is transferable to 4 inches Multi- wafer reactors.

CONCLUSION

In our intensive engineering development, we worked on low cost alternative substrate solutions for III-N materials, for which two contradictory objectives have been tackled:
-Lower the substrate cost of High End solutions based on semi-insulator SiC bulk
-Improve the performances of low end silicon based solutions

Our GaN piezo-electric structures are grown by MBE technique on high resistivity low cost silicon substrates up to 4 inches. Different Epi-structure standards have been developed regarding the mobility, the thickness and the Al content of the active layers. These structures have demonstrated excellent DC and RF characteristics. As reported recently by communications, our material is considered as the state of the art. Other studies have been extended for the reliability tests, which is the next achievement to transfer this engineering development to production.
A roadmap, based on the development of new engineered wafers will be presented. It addresses our solutions to optimize the thermal management budget, minimize the dislocation level and improve the device's performances.

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