

Investigation of Semi-Insulating SiC Wafers Using Contactless Topographic and Temperature-Dependent Resistivity Analysis

Wolfgang Jantz, Stefan Müller and Rudolf Stibal

Semimap Scientific Instruments GmbH
Tullastr. 67 D79108 Freiburg
email wolfgang.jantz@semimap.de phone *49 761 5577878

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Abstract

Semi-insulating SiC substrates originating from different vendors are analysed with nondestructive techniques. Contactless resistivity mapping (COREMA) provides full wafer images of the resistivity ρ in the range $1 \times 10^5 - 1 \times 10^{12} \Omega\text{cm}$. Based on this room temperature pre-characterization particular spots on the wafer are selected for measurement of the temperature dependence $\rho(T)$ to obtain the local carrier activation energy. We find that it varies widely and may be quite different even if ρ values are comparable. Hence both quantities must be measured to obtain a meaningful electrical analysis of semi-insulating SiC. For wafers with persistent conductivity at room temperature the heating curve shows a complex behaviour reflecting the heat-stimulated recombination of centers which are persistently ionized at room temperature.

Introduction

The unique electrical material properties of SiC, including large bandgap, high breakdown voltage and high thermal conductivity, are appealing for high speed, high power microwave applications. Substrates to be used for device fabrication by epitaxy or ion implantation must be semi-insulating, a property realized by the compensation process. It ensures that the Fermi level is pinned near midgap at a partially ionized deep center. Such centers are generated either by intentional doping (e.g. vanadium) or by controlled introduction of a native defect [1]. The

absolute value, temperature dependence and lateral homogeneity of the resistivity ρ critically depends on the concentrations of the defects participating in compensation (shallow donors, shallow acceptors and deep centers) [2]. Successful crystal growth development and process control demands that these quantities are routinely assessed with analytic techniques meeting the requirements of industrial material fabrication.

Experimental Procedures

The contactless capacitive full wafer evaluation with the system COREMA-WT generates highly resolved images of the absolute values and lateral variations of the resistivity ρ at room temperature in the range 1×10^5 to $1 \times 10^{12} \Omega\text{cm}$ [1,3]. The data are obtained with a capacitive parallel plate sensor sequentially probing a 1 mm diameter spot of the wafer material. After sensor positioning by the mechanical scanning unit, a voltage step induces a time dependent charging of the sample and air capacities of the sensor. As shown in Fig. 1, the charge transient exhibits a step Q_0 , an exponential increase with time constant τ and an asymptotic value Q_∞ . The local ρ is calculated with these quantities. Upon scanning a wafer cut from material which is *homogeneous* within the 1 mm diameter area below the sensor, the transient is monoexponential and only τ varies upon scanning. If an increase of Q_0 is observed, part of the probed material is below range ($1 \times 10^5 \Omega\text{cm}$), while a decreasing Q_∞ indicates that part of the probed material is above range ($1 \times 10^{12} \Omega\text{cm}$). A multiexponential transient indicates that the probed material contains two or more intermixed phases with ρ values within the measurable range [4]. By scanning the capacitive sensor across the wafer area, a full wafer ρ topogram and a volume topogram of the

percentage of the measurable material is generated.

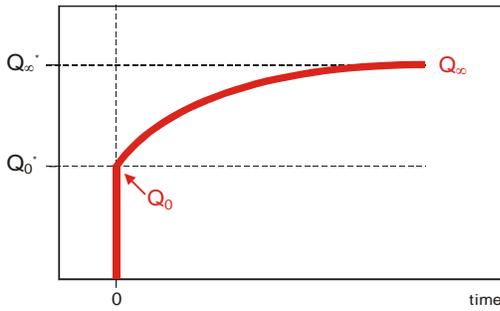


Fig.1 Charge transients observed after application of a voltage step to the capacitive probe of COREMA-WT.

Based on the topographic pre-characterization, the temperature dependence $\rho(T)$ variation of ρ is recorded at individually selected spots with the system COREMA-VT. It contains a capacitive probe designed for high temperature operation, and a temperature control unit presently allowing measurements up to 350 °C. The ρ data are generated quasi-continuously while the sample is cooling in the dark, starting with the maximum temperature. This ensures best possible suppression of eventual persistent conductivity (PC), generated by ambient illumination prior to the measurement (see discussion below). The local activation energy E_a is deduced from the slope of the Arrhenius plot of ρ versus $1000/T$.

Results

Fig. 2a shows a quadrant of the ρ topogram of a 2" SiC wafer. It is semi-insulating across the entire area, in particular does not contain localized semiconducting spots, as do occur rather often in wafers which are seemingly semi-insulating according to a local measurement, but contain defects of e.g. the crystal structure. The smooth radial ρ variation ranges from $7 \times 10^{10} \Omega\text{cm}$ in the center up to $1.8 \times 10^{11} \Omega\text{cm}$ near the margin. The histogram given at the right side further illustrates and quantifies the ρ distribution. Such topograms are typically obtained for state-of-the-art wafers generated by well controlled crystal growth, doping and wafering processes. The corresponding volume topogram (Fig. 2b) further corroborates that the material is locally homogeneous, i.e. does not contain phases with a resistivity different from that

shown in Fig. 2a. Again, this finding is an important additional result of the detailed COREMA analysis and is by no means self-evident.

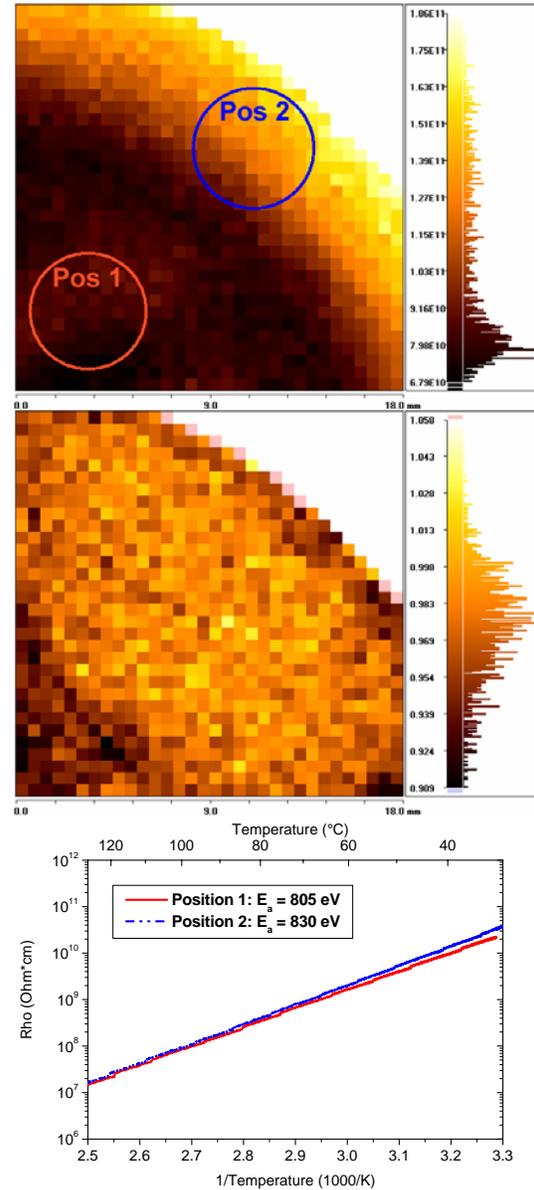


Fig. 2 Characterization of a state-of-the-art semi-insulating SiC wafer: Resistivity topogram (top), volume topogram (middle) and temperature dependence of resistivity (bottom) measured at sample spots marked (1) and (2) on the ρ topogram.

Fig. 2c shows $\rho(T)$ in Arrhenius plot form, measured at positions indicated (1) and (2) in Fig. 2a. The slopes of the curves are virtually identical and the vertical displacement at RT agrees with the different absolute values of the ρ topogram at the measured spots. The perfect exponential dependencies over a wide tempera-

ture range confirm that the compensation process is well defined across the wafer, involving the same deep center with a gradually varying degree of compensation-induced ionization. The activation energies of 805/830 meV are indicative that the sample has been doped with vanadium.

The $\rho(T)$ data shown in Fig. 3 pertain to a wafer with extremely high resistivity at room temperature, well beyond the upper range limit $1 \times 10^{12} \Omega\text{cm}$ of COREMA-WT. However, by heating the sample to $T > 225 \text{ }^\circ\text{C}$, ρ is lowered into the measurable range. The activation energy $E_a = 1490 \text{ meV}$ obtained with $\rho(T)$ data between 250 and $360 \text{ }^\circ\text{C}$ allows to extrapolate to $\rho(300\text{K}) \approx 10^{21} \Omega\text{cm}$.

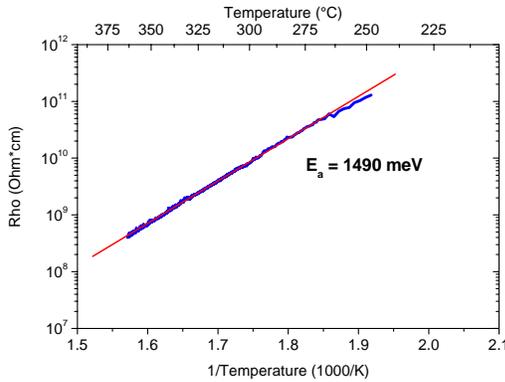


Fig 3 Temperature dependence and activation energy of a SiC wafer with very high resistivity (around $10^{21} \Omega\text{cm}$) at room temperature.

The results presented in Figs. 2 and 3 convincingly show that, for well defined material, COREMA-VT yields a linear Arrhenius plot for resistivities up to $10^{11} \Omega\text{cm}$ and temperatures up to 600 K. It is, therefore, well suited for routine production wafer control. Moreover, as shall be demonstrated now, it may serve to analyse exploratory material in order to improve crystal growth and wafer fabrication processes.

In Fig. 4a, the ρ topogram of such exploratory wafer material is shown. The peculiar radial variation pattern and a strong PC, as further discussed below, indicate that, in spite of the satisfactorily high $\rho(300\text{K})$ in the $10^{10} \Omega\text{cm}$ range, the various doping and defect concentrations influencing the compensation process are not fully under control. This suspicion is strongly substantiated by the $\rho(T)$ measurement shown in Fig. 4b. As distinct from the data presented in

Fig. 2, in spite of comparably high resistivity, the $\rho(T)$ behaviour is quite different. Up to $T = 175 \text{ }^\circ\text{C}$, it is governed by a very small $E_a = 250 \text{ meV}$, whereas for higher T one measures $E_a = 950 \text{ meV}$. These observations may be understood by postulating two energy levels, the shallow one strongly ionized by compensation already at room temperature to account for the high resistivity. Upon heating, it eventually becomes *fully* ionized. As a result, the Fermi level drops down to the deeper level, whence $\rho(T)$ is then controlled by the higher activation energy. The steps in the Arrhenius curve are artefacts of the sweep time optimization which appear only if the transient is not monoexponential, hence indicate that the material is locally inhomogeneous.

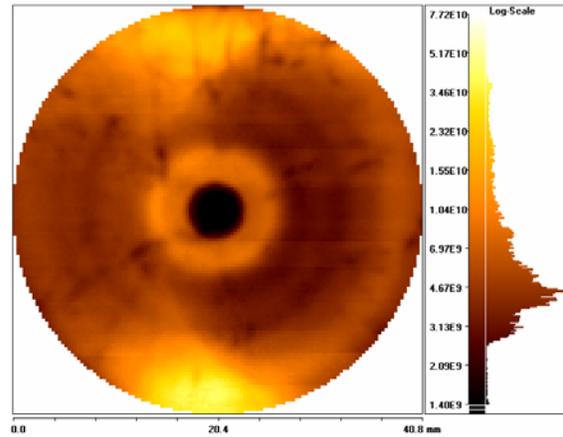


Fig 4a

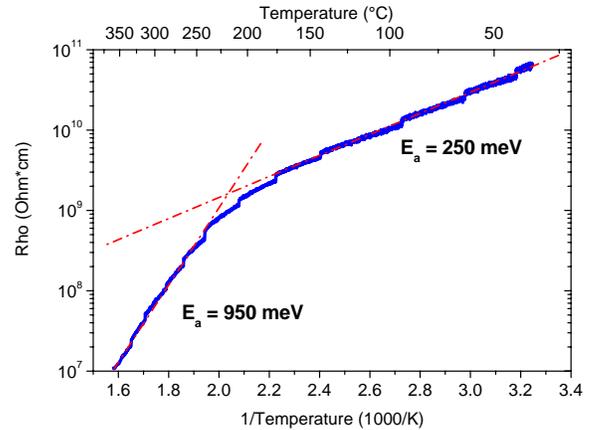


Fig 4b

Fig. 4 ρ topogram and temperature dependence of an exploratory SiC wafer with two different activation energies.

As mentioned, the $\rho(T)$ data are obtained by letting the sample cool down in the dark, because, after positioning and shielding it

from ambient light, the first heating curve is influenced by eventual PC. This is shown in Fig. 5 for the same wafer and sample spot of Fig. 4 a,b. It is seen that the expected exponential decrease of $\rho(T)$ is observed only after a maximum at $T = 250$ °C has been surpassed. This observation is readily understood by assuming that a persistently ionized center (i.e. a center which, upon ionization, reconfigures to build a barrier against recombination) is neutralized by T-stimulated recombination. Such behaviour is closely related to thermally stimulated luminescence and DLTS; hence the measured $\rho(T)$ peak may be used to define, identify and eventually eliminate the persistently conducting defect center.

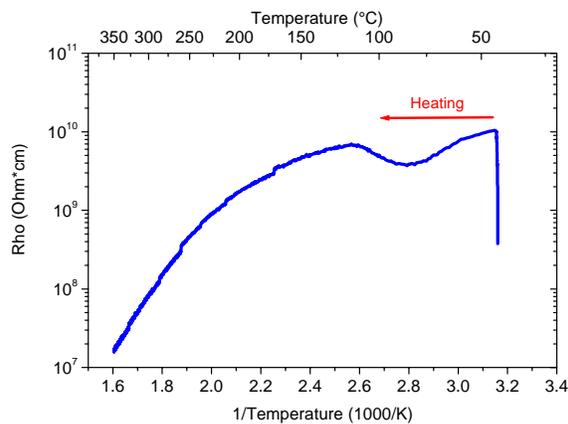


Fig.5 Initial temperature dependence (heating curve) of a wafer exhibiting instantaneous increase of resistivity upon shielding it from ambient light, and subsequently heat-stimulated decay of persistent photoconductivity.

Conclusion

The combination of topographic and temperature-dependent resistivity measurements yields a detailed electrical characterization of semi-insulating SiC wafers. The presented results demonstrate that the analytic instruments are useful for both routine production control and for detailed physical investigation of exploratory material and fabrication processes.

References

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Acronym list

COREMA: COntactless REsistivity MEAsurement

DLTS: Deep Level Transient Spectroscopy

PC: Persistent Conductivity