Evaluation of 4” InP Substrates for Epi-Ready Production MBE Growth

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Abstract

4-inch diameter semi-insulating InP substrates from multiple suppliers were evaluated and compared in terms of their epi-readiness as required for production molecular beam epitaxy. All epiwafers in this work exhibited excellent crystalline and structural properties, and the electrical properties were consistent from vendor-to-vendor. The post-growth surface morphology and defect density were typically within standard expectations; however, occasionally some fallout was observed due to variations in substrate surface finish, unrelated to the epi-growth. Significant differences in epilayer-substrate interfacial properties were observed between the various vendors and also within substrate lots from individual vendors. While some substrates exhibited a clean interface, others had n-type charge accumulations of varying magnitudes. The interface contamination, silicon or sulfur arising from the substrate surface preparation process or from the substrate packaging, can lead to poor device isolation.

INTRODUCTION

InP-based semiconductor devices are key components for the next generations of wireless and optical telecommunications infrastructure that require extremely high frequency electronic capability. The performance advantage and commercial acceptance of InP-based optoelectronic integrated circuits is driving the technology toward manufacturing goals of increased volume at reduced cost. Critical to achieving this is the InP substrate itself, where greater demand will require consistent, high quality wafers in larger diameters. Currently, most InP-based HEMT and HBT circuits are fabricated on epiwafers grown by molecular beam epitaxy (MBE) or metal-organic chemical vapor deposition (MOCVD) on Fe-doped semi-insulating (SI) InP substrates. While several manufacturers are developing 6-inch diameter InP substrate capabilities [1], the industry standard is 4-inch diameter. Large diameter InP single crystals are grown using several techniques [2–6]: liquid encapsulated Czochralski (LEC), vapor pressure controlled Czochralski (VCZ), vertical gradient freeze (VGF), and vertical boat (VB). Until 2003, only one or two suppliers could meet the 4 in. substrate specifications required by the integrated circuit manufacturers, but currently substrates are available in the market from at least six different vendors. However, the quality of these substrates is still not as consistent as their GaAs counterparts. In particular, the unique epi-ready process of each vendor contributes to variability in the post-epitaxial-growth surface finish, with observed inconsistencies both from vendor-to-vendor and even within shipments from individual vendors. For the substrate manufacturers, etch pit density (EPD) is a key metric for evaluating substrate quality. In fact, reducing EPD has been the driving force behind the development of the various crystal growth techniques, as the old standard LEC resulted in very high densities (typically >50,000 cm^{-2}). Guaranteed average EPD values in production quantities of 4 in. SI InP substrates have dropped from <10,000 cm^{-2} in 2001 (achieved only by VGF) to < 5000 cm^{-2} in 2004 (using VGF, VB and VCZ), and further improvements should continue the trend.

In this paper, we compare 4 in. diameter SI InP substrates from five major suppliers in terms of epi-readiness for MBE growth. Substrate property requirements for MBE are different than MOVCD, where an *in-situ* hydrogen cleaning process can sometimes overcome variations in substrate surface properties. For this MBE study, generic lattice-matched InP-HEMT and HBT structures were grown. The epiwafers were evaluated in terms of their structural properties, surface morphology, and the epilayer-substrate interface quality and cleanliness. Additionally, some epiwafers were processed into large-area devices to evaluate the impact of the substrates on dc performance.

EPIWAFER GROWTH AND CHARACTERIZATION PROCEDURES

The epitaxial growths in this study were all performed in an Oxford Instruments Thermo-VG V-100 MBE system. The V-100 utilized standard solid-source group III effusion cells and group V arsenic and phosphorous valved-crackers. Multi-wafer growths were carried out in a 3×4” configuration, allowing for direct side-by-side comparison of nominally identical substrates from different vendors via a single growth run. The 4 in. diameter SI InP epi-ready substrates, supplied by five different manufacturers hereafter referred to as Vendors A – E, were loaded into the MBE system directly from the vendors’ packaging. The quality of

the substrates was compared using two basic device structures: a single pulse doped InP-HEMT with a lattice-matched InGaAs channel, and a double HBT with a C-doped InGaAs base and InP emitter and collector layers.

Various techniques were used to evaluate the epiwafers and the underlying quality of their substrates. High resolution x-ray diffraction (XRD) probed the structural quality of the crystal layers. HEMT transport properties were measured at 300 K and 77 K by Hall effect in the van der Pauw geometry. Large area transistor devices were fabricated and their dc characteristics were measured. Two key epiwafer properties were the surface morphology and the epilayer-substrate interface cleanliness. The surface morphology was compared using a Tencor Surfscan 6220, which nondestructively maps and quantifies the light-point defects across the wafer surface. The interface charge properties were investigated using an Accent Polaron electrochemical capacitance-voltage (E-CV) measurement system. This was corroborated by in-house buffer layer current leakage measurements using 200 µm wide contacts with 2 µm mesa separation.

INP SUBSTRATE COMPARISONS

Several epiwafer properties were reproducible for identical structures grown on substrates from each of the five vendors. The XRD (004) rocking curves of InP-HEMTs and HBTs consistently showed sharp peaks and distinct thickness fringes, indicative of good crystalline and structural properties of the epilayers and their underlying substrates. For example, an InP-HEMT structure grown on substrates from Vendors A – C in a single growth run produced nearly indistinguishable XRD spectra (not shown). Hall measurements on the 200 Å InGaAs channel InP-HEMT structure typically resulted in a channel charge around 3×10^{12} cm^{-2} and mobility values of 10,000 and 40,000 cm^2/V-s at 300 K and 77 K, respectively. The transport properties were nominally the same for growths on substrates from Vendors A – E. Interestingly, the interface charge contamination seen on some of the substrates (see below) had no correlation with the Hall data, indicating that the Hall measurement was dominated by the channel.

Large area DHBT devices fabricated for dc testing also showed very comparable results across the different substrate vendors. Gummel plots overlapped for DHBTs from wafers grown in a single run in the 3×4" configuration. The data with the most variation was the figure of merit, gain (β) divided by base sheet resistance. This was probably due to vendor-to-vendor variations in the actual substrate growth temperature, even though all 3 wafers in a given run were heated identically. This slight temperature difference probably was due to differences in crystalline structure (different substrate boule growth methods) or in Fe-doping concentration required to make the substrates SI. The temperature variations affect the base C-doping activation, which resulted in the figure of merit shifts from wafer to wafer. The consequence of this observation was that temperature settings for the growth of a given HBT structure needed to be individually adjusted and optimized for each substrate vendor.

The surface morphology, a key parameter in assessing epiwafer material quality, was evaluated by defect density measurements using the Surfscan 6220. The multiwafer MBE configuration, where substrates from different vendors were grown side-by-side, aids the evaluation of the substrates by allowing growth or system related defects to be differentiated from substrate related ones. A wide variety of Surfscan defect maps are shown in Figure 1. Typically, defect maps showed a random, uniform distribution across the epiwafer surface, as seen in Fig. 1(a) and 1(b) for growths on substrates from Vendor B and C, respectively. However, occasionally other patterns emerge which were related to substrate EPD or surface preparation problems as decorated and revealed by the epilayer growth cycle. Figure 1(c) is an extreme example of the case where the epi-growth exposes the high EPD of the underlying substrate from Vendor A. The other two wafers in that exact same growth run, from Vendors C and D (defect maps not shown), had uniform distributions and had defect densities two orders of magnitude lower. Vendor A used a variant of LEC for its crystal growth while the other wafers were VCZ or VB, and LEC is known for its higher EPD values [2, 3, 6].

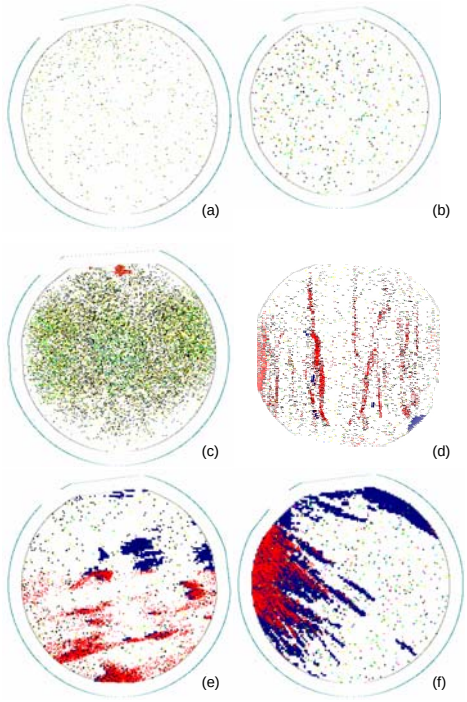

Figure 1. Surfscan 6220 defect maps for InP-HBT structures grown on substrates from (a) Vendor B, (b) Vendor C, (c) Vendor A, (d) Vendor D, (e) and (f) Vendor C. The maps compare uniform distributions typical of MBE (a, b) with unusual defect patters related to substrate problems (c – f).

The non-uniform defect maps of Fig. 1(d, e, f) are examples of unusual patterns related to surface preparation irregularities. These substrates were from Vendors C and D. The hazy areas around the wafer edges and, especially, the directionality of the streaky patterns appear possibly related to non-uniform interaction with a wet chemical treatment flow or drying process in the substrate manufacturing. These features were not curved scratch-like marks as may be formed during substrate polishing [7], but rather were accumulations of defects or local areas of abnormal growth roughness. IQE has worked with the substrate vendors to perform experiments on variations in their epi-ready surface preparation process. The surface could be deliberately changed via different treatments, and growths on such experimental substrates showed surfaces ranging from no morphological pattern to streaks to complete milky haze. One curious phenomenon was that the haze and streak patterns were more prevalent on, but not limited to, substrates with flat orientations that were not US (i.e. EJ or other non-standard flat orientations). The wafers in Fig. 1(d, e, f) all had non-US flat orientations, compared to Fig. 1 (a, b, c) which were US orientation flats. We speculated that the vendors' substrate process may have been developed for US flats, which are the prevalent standard for 4" SI InP, and that when using the same process for substrates with different flat orientations there was a detrimental interaction between the process and the position of the flats. We continue to work with the vendors to investigate these interactions, and while improvements have been made occasional outliers still occurred.

The cleanliness of the interface between the substrate and the epilayer was investigated using Polaron E-CV and buffer layer leakage current measurements. A contaminated interface may be detrimental to circuitry due to changes induced in device performance or to an inability to achieve proper on-chip device isolation. Polaron revealed any problems via an accumulation of charge at the interface. This accumulation could be epitaxy-related or substrate related. However, since the substrates were loaded directly from the incoming packaging into the MBE chamber, any interface differences observed between wafers from a single growth run were definitively attributed to the substrates. Figure 2 shows the E-CV measurements for two separate InP-HEMT growth runs, demonstrating clear variations in interface cleanliness due to differences in the InP substrates. The interface had no charge at all for Vendor A in Fig. 2(a), while Vendor C showed a minor bump and Vendor B had a large charge spike. In all E-CV measurements, the interface charge was n-type. The leakage current measurements scaled with the E-CV peaks, with current ratios of 1:3000:300,000 for Vendors A:C:B, respectively, in Fig. 2(a). Interface contamination variability was also observed within individual substrate vendors, as seen for the two Vendor C wafers in Fig. 2(b).

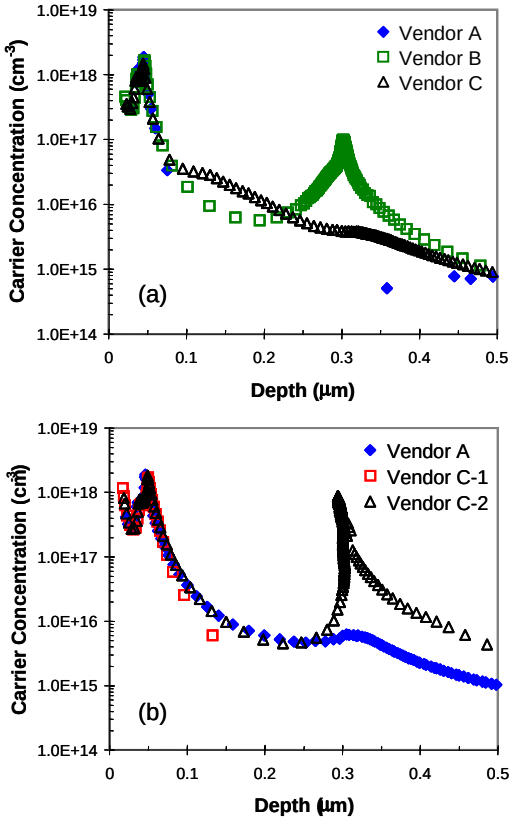

Figure 2. Polaron E-CV plots of two separate, (a) and (b), LM-HEMT growths in the 3 × 4 in. configuration. The charge peak seen at the left, near the epiwafer surface, in all six samples is from the Si atomic planar doping and the InGaAs channel. The peak seen at a depth of 0.3 µm in some of the samples is due to a charge accumulation at the epilayer-substrate interface.

From measurements over the past two years, Vendor A rarely has shown any interface charge, while Vendor B always has exhibited well defined interface charge peaks and leakage current. Vendor C has shown the most variability, ranging from no interface charge to large charge peaks, although typically Vendor C had small amounts of charge and its leakage currents were closer to that of Vendor A than Vendor B. With minimal data points to date, Vendors D and E showed low interface charge via E-CV, and had leakage currents higher than Vendor A and comparable to the best of Vendor C. Standard secondary ion mass spectroscopy (SIMS) on InP-HEMT epiwafers was used to investigate the nature of the interface charge, and the substrate vendors often quote time-of-flight SIMS [8] when analyzing their surface contaminants. Silicon and sulfur appear to be the main electrically active culprits. Substrate-related causes of the interface charge would be either from the final surface preparation by the manufacturer (e.g. water, chemicals, or equipment) or from the packaging in which the substrates were stored and/or shipped. Our substrate preparation experiments with the vendors have had mixed results with respect to interface charge. One vendor seemed unable to

change the charge peak even with different treatments, while for other vendors variations in chemical treatment seemed to affect the interface charge, although not always reproducibly. Since other factors not related to direct surface processing may influence the cleanliness, this problem has been difficult to isolate.

CONCLUSIONS

The quality of 4 inch diameter SI InP substrates from multiple suppliers was compared in terms of their epi-ready properties for MBE growth. XRD demonstrated excellent crystal quality for epiwafers grown on substrates from all vendors. Hall measurements on InP-HEMTs were nominally identical for all vendors, and the transport properties appeared to be insensitive to the presence of the interface charge accumulation. Similarly, the DHBT dc parameters were very comparable for structures grown on substrates from each vendor. The surface morphology showed variability even within individual vendors. For the most part, epiwafers from all vendors showed uniform defect distributions within acceptably low density ranges. However, occasionally some outliers occurred with random defect or haze patterns related to substrate EPD or surface preparation. During standard product lots of HEMTs and HBTs, this random variability in surface morphology has caused some yield loss. The cleanliness of the epilayer-substrate interface also showed considerable variability between vendors and even within substrate lots from some vendors. Multiple experiments have shown accumulations of n-type charge, over a wide range of concentration levels, at this interface. Large interface charge resulted in buffer leakage which would be detrimental to integrated circuits due to poor device and circuit isolation. The prime contaminants have been identified as S and Si, which may arise on the substrate during surface cleaning and preparation or may come from the packaging materials. We are working with our substrate vendors to better understand and eliminate this periodic problem. Overall, the quality of the standard 4" InP substrates available on the market is very good, and has improved in last two years. Previously, only one or two suppliers were qualified for our InP HBT and HEMT epiwafer production, but now there appears to be at least four viable options. Continued improvement in the consistency of surface morphology and contamination is needed for InP-based epiwafer and integrated circuit production to move into a higher volume manufacturing process.

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REFERENCES

[1] T. Sato, K. Aoyama, K. Sato, S. Numao, I. Honma, S. Sugano, T. Hoshina, and K. Iwasaki, Technical Digest of the 2002 Compound Semiconductor Manufacturing Expo (CS-MAX 2002), San Jose, Nov 2002, p. 220.

[2] R. Ware, Proceedings of the 13th International Conference on Indium Phosphide and Related Materials, Nara, Japan, 2001, p. 121.

[3] T. Kawase, N. Hosaka, K. Hashio, and Y. Hosokawa, Proceedings of the 16th International Conference on Indium Phosphide and Related Materials, Kagoshima, Japan, 2004, p. 589.

[4] Noda, M. Nakamura, A. Arakawa, and R. Hirano, Proceedings of the 16th International Conference on Indium Phosphide and Related Materials, Kagoshima, Japan, 2004, p. 552.

[5] U. Sahr and G. Muller, Proceedings of the 12th International Conference on Semiconducting Materials (SIMC-XII), 2002, p. 13.

[6] K. Hashio, N. Hosaka, S. Fujiwara, T. Sakurada, and R. Nakai, Proceedings of the 15th International Conference on Indium Phosphide and Related Materials, Santa Barbara, CA, 2003, p. 542.

[7] D. Clark, Technical Digest of the 23rd Annual GaAs IC Symposium, pp. 181-184, 2001.

[8] N. Thomas, G. Jacob, and H. Hardtdegen, Proceedings of the 10th International Conference on Indium Phosphide and Related Materials, pp. 96-99, Tsukuba, Japan, 1998.

ACRONYMS

HEMT: High Electron Mobility Transistor
HBT: Heterojunction Bipolar Transistor
MBE: Molecular Beam Epitaxy
MOCVD: Metal-Organic Chemical Vapor Deposition
SI InP: semi-insulating indium phosphide
LEC: liquid crystal Czochralski
VCZ: vapor pressure controlled Czochralski
VGF: vertical gradient freeze
VB: vertical boat
XRD: x-ray diffraction
E-CV: electrochemical capacitance-voltage
SIMS: secondary ion mass spectroscopy