

# InP Backside Via Formation Using High Etch Rate and Low Temperature HI-Based ICP Etching

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## Abstract

InP-based devices have shown great potential in realizing high-speed Monolithic Millimeter-wave Integrated Circuits (MMICs). Backside via is one of the most important elements for high-speed MMICs. We have demonstrated high etch rate and low temperature InP etching using HI-based Inductively Coupled Plasma (ICP). A Dry Film Resist (DFR) with high temperature tolerance was employed as an etching mask. Using these technologies, InP backside via formation process was simplified. After via formation, electric properties were evaluated over a 3-inch diameter wafer. High uniformity and reproducibility enough for practical applications were obtained.

etching using another gasses. By using HBr gas and a photoresist mask, high etch rate of 1.5  $\mu\text{m}/\text{min}$  was reported [5].

In this paper, we present a novel via formation technology that uses HI-based ICP and a DFR. The etch by-product,  $\text{InI}_x$  has higher volatility at lower temperatures and the DFR has high temperature tolerance. An average InP etch rate of 1.6  $\mu\text{m}/\text{min}$  with smooth etching surface was obtained at a low wafer temperature of 140 °C. Using this etching technology, we simplify backside via formation process and improve uniformity of via properties over a 3-inch diameter wafer and reproducibility.

## EXPERIMENT

The backside process flow is shown in Fig. 1. The first

## INTRODUCTION

Owing to their excellent properties, such as ultra-high speed and low power consumption, InP-based heterojunction bipolar transistors (InP HBTs) [1] and high electron mobility transistors (InP HEMTs) [2] are promising to realize high-frequency and high-performance MMICs. The backside via is essential for MMIC technology, because it provides significant advantages, *i.e.*, a low parasitic inductance and a low access resistance to the grounding plane, and serves as a heat dissipation path.

For higher frequency applications, accurate control of via properties becomes to be very important. To form deep vias into InP, high etch rate etching with vertical sidewall is required.  $\text{Cl}_2$ -based dry etching technologies are usually used [3, 4] for InP etching. Because of the low volatility of etch by-products of  $\text{InCl}_x$ , high wafer temperatures around 200 °C are needed to obtain acceptable etch rate and enough vertical sidewall profile for high aspect ratio via formation. In the case, a dielectric or metal mask that can endure high temperature is used. But this complicates backside via formation process and causes large variation of via size and properties. There are a few approaches for InP backside via

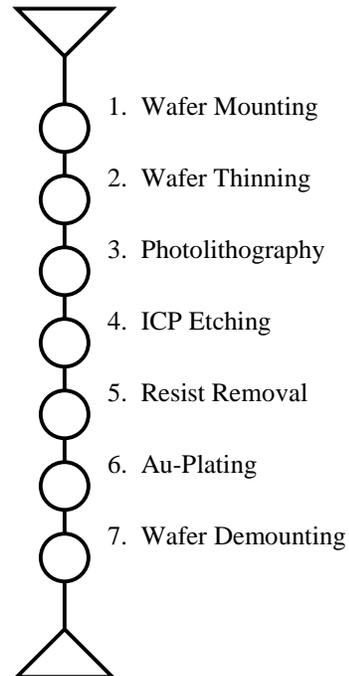


Fig.1. Backside via process flow.

step is wafer mounting and thinning. A frontside processed 3-inch diameter InP wafer is mounted on a carrier by wax. Then the wafer is thinned to 100  $\mu\text{m}$  using a combination of grinding and polishing techniques.

The next step is photolithography. A negative-type 40  $\mu\text{m}$ -thick DFR is used. The DFR is laminated on the InP wafer and patterned by a standard photolithography technique without hard baking. Then InP is etched by HI-based ICP. A 13.56 MHz ICP source is used to generate a high density plasma. Ion energy at the wafer surface is controlled by biasing the cathode at 13.56 MHz. The wafer is clamped mechanically on the cathode with He backside cooling. To form high aspect ratio vias, we optimized the HI total flow, total pressure, and wafer temperature. An average etch rate of 1.6  $\mu\text{m}/\text{min}$  and a selectivity of InP to resist mask of 15 were obtained under the ICP plasma conditions of 90 sccm HI, 60 sccm He, 7.5 sccm  $\text{SiCl}_4$ , 120  $^\circ\text{C}$  chamber temperature, 3.0 Pa total pressure, 700 W ICP power, and 55 W bias power.

The distribution of etch rate and angle of the via sidewall across a 3-inch diameter wafer are shown in Fig. 2 (a) and Fig. 2 (b), respectively. Figure 2 (c) indicates position of measured points. As shown in these figures, very uniform etching is realized. The uniformity of etch rate and angle of the via sidewall are 3.3 % and 2.1 %, respectively. The selectivity of InP to frontside metal is over 20. So the etching is easily stopped at the frontside metal stack over a 3-inch diameter wafer.

Figure 3 shows size dependence of the via etching. As shown in this figure, all vias have good profiles and smooth surfaces. The size dependence of the etch rate is small [5], which is only 8 % reduction from 100  $\mu\text{m}$  to 60  $\mu\text{m}$  via diameter. This result shows that our etching technology is suitable for higher aspect ratio via formation.

The next step is resist removal. Due to the low temperature etching, the DFR can easily be removed after the etching. After removal of the DFR,  $\text{O}_2$  and  $\text{CF}_4$  plasma treatment is performed.

The last step is Au electro-plating and wafer demounting. A seed metal layer of Pt/Au was sputtered and

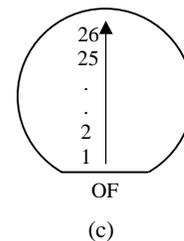
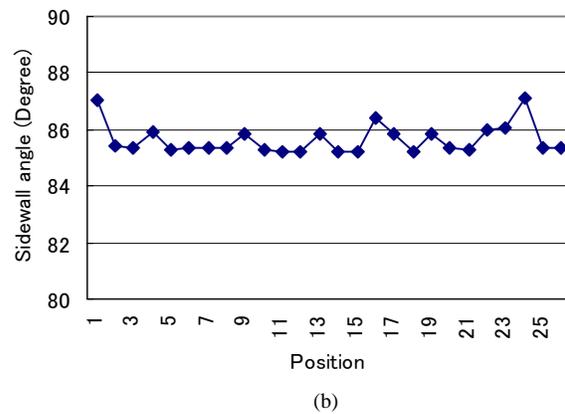
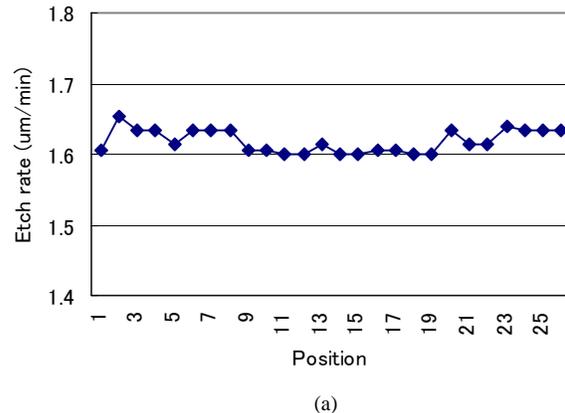


Fig.2. Via etching uniformity. (a) Etch rate, (b) Sidewall angle, (c) Measured positions

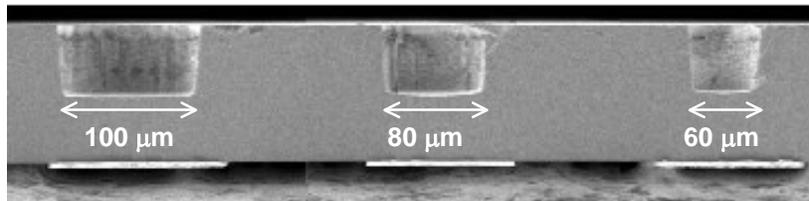


Fig. 3. Cross-section of via after etching. The diameters of the via are 100  $\mu\text{m}$ , 80  $\mu\text{m}$ , and 60  $\mu\text{m}$ , respectively. All vias are etched at the same time.

then Au was plated. To improve the uniformity of plated Au thickness in the vias, we optimized the plating current and plating liquid flow condition. Figure 4 shows a cross-section of the InP backside via after Au plating. The diameter at the opening of the via was 80  $\mu\text{m}$ . Via etching was stopped at the frontside Au stack and the thickness of plated Au was 15  $\mu\text{m}$ . Figure 5 shows a top surface view of the via. After the Au-plating process, the wafer was demounted and then cleaned in a solvent bath and exposed to  $\text{O}_2$  plasma.

### EVALUATION OF BACKSIDE VIA

To evaluate InP backside via properties, we formed via test patterns over a 3-inch diameter wafer. In this test pattern, via is placed at the center of a frontside Au stack with 100  $\mu\text{m}$ -width rectangular shape and the stack is connected to measurement pads. From *s*-parameter measurements, the inductances of 12.9 pH and 16.7 pH were extracted for the vias with 80  $\mu\text{m}$  and 60  $\mu\text{m}$  diameters, respectively. These values coincide very well with simply estimated via inductances of 12.7 pH and 16.1 pH, respectively [6]. We investigated uniformity and reproducibility of the via inductance. Figure 6 shows distribution of 80  $\mu\text{m}$  diameter via inductance over a 3-inch diameter wafer. The average and standard deviation of via inductance were 13.2 pH and 0.3 pH, respectively. Figure 7 shows the trend of via inductance. All wafers hit almost the target value and the variation of via inductances over 5 wafers was only 1.1 pH.

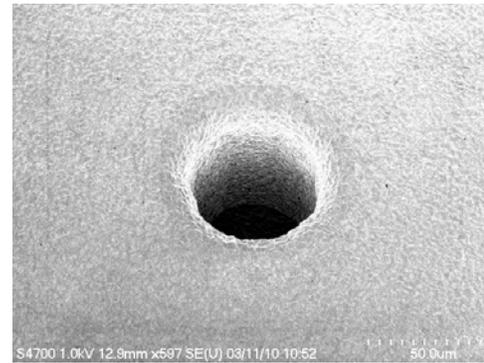


Fig. 5. SEM photograph of InP backside via after Au plating. Diameter at opening is 80  $\mu\text{m}$ .

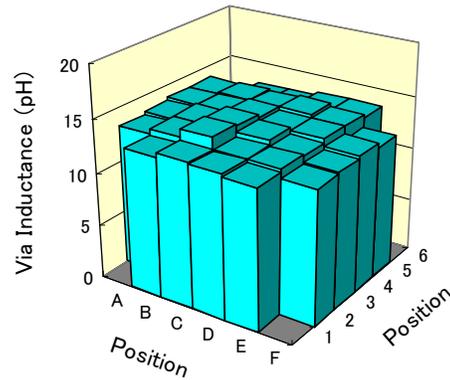


Fig. 6. Distribution of 80  $\mu\text{m}$  diameter via inductance over a 3-inch diameter wafer. The number of tested sample is 32.

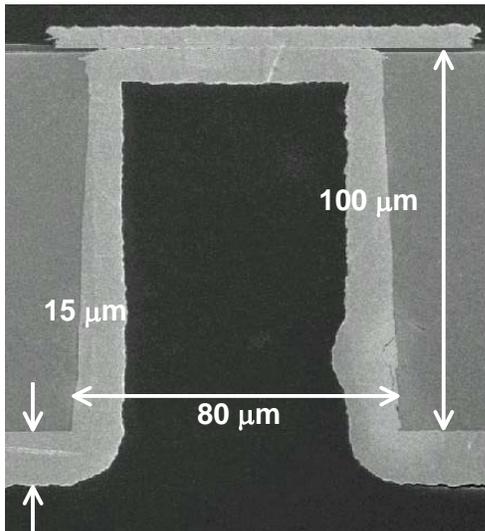


Fig. 4. Cross-section of InP backside via after Au plating. The depth is 100  $\mu\text{m}$  and the diameter at the opening is 80  $\mu\text{m}$ . 15- $\mu\text{m}$  thick Au is plated.

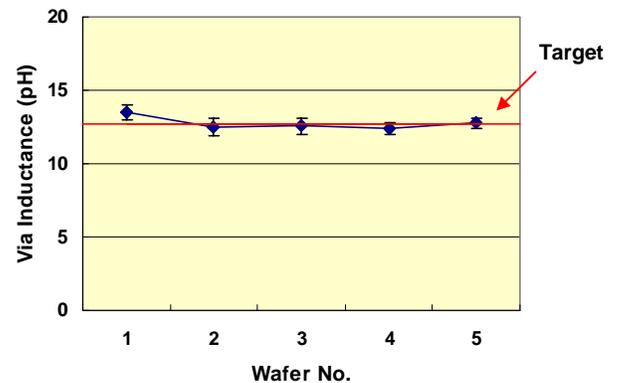


Fig. 7. Trend of 80  $\mu\text{m}$  diameter via inductance.

## RELIABILITY

A heat cycle test under a condition of temperature cycling from 150 °C to -65 °C was carried out. Test chip was soldered on Au coated ceramic submount using AuSn preform at 320 °C. The number of tested sample was 60. After testing of 100 cycles, no vias were deformed. These results promise that our InP backside via process is available for practical applications.

## CONCLUSIONS

We have successfully demonstrated InP backside via formation using high etch rate and low temperature HI-based ICP etching. An average InP etch rate of 1.6  $\mu\text{m}/\text{min}$  and selectivity of InP to a resist mask of 15 at a wafer temperature of 140 °C were obtained. The uniformity of etch rate and sidewall angle were very high over a 3-inch diameter wafer. From *s*-parameter measurements, the inductances of 12.9 pH and 16.7 pH were extracted for the vias with 80  $\mu\text{m}$  and 60  $\mu\text{m}$  diameters, respectively. The trend of 80  $\mu\text{m}$  via inductance over 5 wafers showed excellent reproducibility. The via has passed the heat cycle test under the condition of a temperature cycling from 150 °C to -65 °C. The results indicate that the via formation process has an enough potential for practical applications.

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