Resistance and Inductance of Through-Wafer Vias: Measurement, Modeling, and Scaling

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Abstract

The measurement of substrate vias (SVIAs) in process control modules and the interpretation of that measurement is reviewed. They are seen to typically have resistances of about 5 mOhms and noisily variable inductances of 10 – 25 pHenry for a nominal 50 um diameter SVIA. Both increase for smaller SVIA diameters.

INTRODUCTION

Bring me to the test,
And I the matter will re-word; which madness
Would gambol from.
- Hamlet. Act iii. Sc. 4.

The test brought to be reviewed here is the difficult measurement of a very low resistance, very low inductance through-wafer vias (substrate vias or SVIAs) which need not lead to madness if done with care and carefully interpreted. We will also describe our efforts to "re-word" (translate) the test onto a much smaller test structure.

SVIAs connect front surface features to backside ground planes. They are commonly used in many current compound semiconductor circuits. Their inclusion in high-performance, high frequency circuits requires a thorough characterization, and ongoing monitoring, of their impedance. We also wish to have an understanding of how the SVIA impedance changes with via size and geometry. Special structures and methods are employed for these purposes, and those are the subject of this report.

SVIA'S AND SVIA TEST STRUCUTURE

TriQuint produces a few variants of SVIA's for its various process families. Fig. 1 shows the two basic types – tapered and "wine glass" (the light area in the wineglass is a cross-section artifact), with the wafers' front sides down in the figure. Both types of SVIA are dry-etched on wafers mounted upside-down on carriers and ground to 100 um thickness. After the holes are cut, plated gold is used as a backside blanket metal, which climbs the SVIA wall to contact a frontside landing pad. After fabrication of SVIAs, the wafers are transferred to saw tape, and tested from the frontside on the tape frame on automated RF test systems.

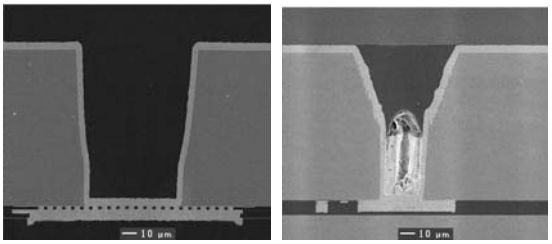

Fig. 1 Tapered and Wine Glass SVIA Cross Sections

Fig. 2 shows the left half of the original TriQuint process control module (PCM) test structure. The SVIA holes are shown as circles, typically 35 – 50 um in diameter when they reach the frontside, and bondpads are shown as crosshatched areas. The frontside landing pads, typically 70 – 120 um wide, are made octagonal to distinguish them from bondpads. This structure covers 0.87 mm^2.

To allow high frequency inductance measurements [1], the module is laid out as a two-port network with a Ground-Signal-Ground on each side for testing with Cascade Microtech Air-Coplanar Probes (ACP). We use 100 um bondpads on a 175 um pitch. 200 um long lines connect the signal pads to the central SVIA, and four SVIA returns come back to the frontside grounds on both sides with shorter lengths of frontside metal.

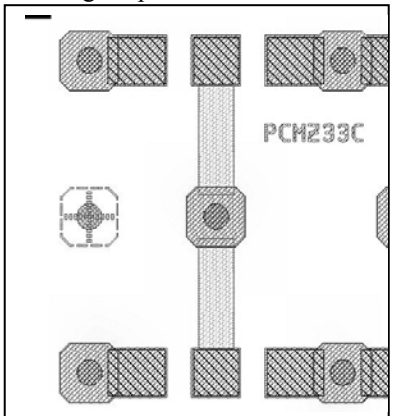

Fig. 2 Large PCM Structure

This version takes up far too much wafer area. Also, calibration is difficult because the large pad – pad space does not match the pitch of the normal Cascade Microtech calibration structure, so probes must be moved after calibration, which is undesirable.

The latest test structure used at TriQuint for this measurement is shown in Fig. 3 (top). At 0.24 mm^2, it is much smaller than previously, and probes need little or no lateral movement after calibration. Differences in values determined from these two structures will be discussed.

Clearly, this is not a simple measurement across an SVIA. Moreover, the low impedance of the SVIA poses

significant measurement challenges. Since the wafer backside is on a saw tape frame at the time of test, electrical access to the backside is only through four additional SVIAs. The bottom of Fig. 2 shows what this structure looks like electrically, with Z3 being the central isolated SVIA we are trying to characterize.

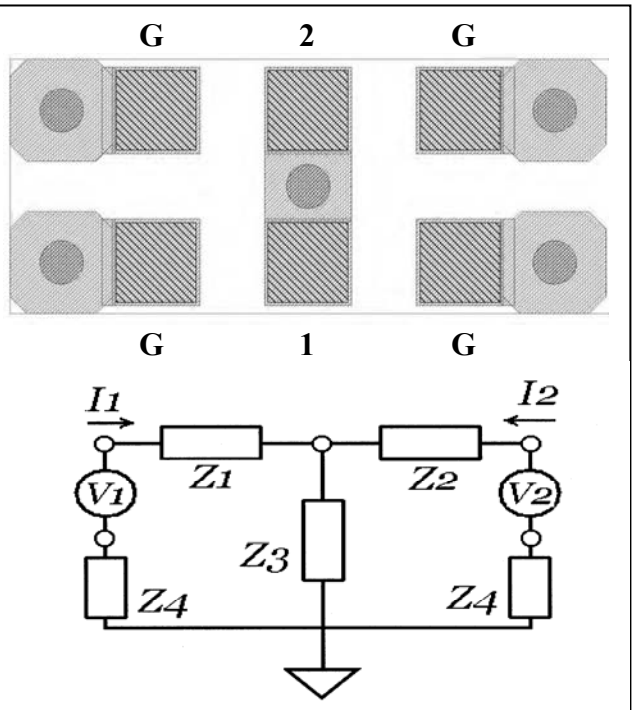

Fig. 3 SVIA Test Structure (top) Layout and (bottom) Schematically (**G** = Common Ground)

TEST METHODS

For measuring resistance, a psuedo-Kelvin test is used. A rather high current (100 mA) is forced into pad 1 and the induced voltage is measured with a high impedance probe at pad 2. This eliminates some of the parasitic resistances, but not those of the return path. It is critical to determine the stray resistance, which can be expected to be larger than the resistance of the SVIA under test. In our case, about 2/3 of the measured resistance of about 30 mOhm is measured if the probes are placed on a blanket sheet of plated gold. Fortunately, that is relatively independent of exact probe spacing, so (for a given set of probes and cables) it can be assumed to be a constant offset resistance. A better method, being added to our new test structures, is a metal short right next to the SVIA structure so the resistance offset can be measured and subtracted at each site.

Additionally, since the "launcher" length in the new test structure is smaller than the pad size, the launcher resistance (Z1 in fig. 2) depends critically on where probe tip 1 is placed on the pad on the "home" site and on how much it varies in that position as you auto-step across the wafer (prober runout error). Forcing current in both sides serially and averaging can compensate for the latter, but careful initial positioning is critical. We measure a difference of as much as 1 mOhm for force probe distance from the SVIA under test varying from closest to furthest away on Pad 1.

And, having corrected for all those sources of error, one needs also to consider that (compared to putting the probes on a frontside sheet of metal) you are not measuring a single SVIA, but rather that SVIA, plus 4 parallel resistors consisting of the resistance through the backside metal to the return SVIA plus an SVIA resistance plus the front side resistance back to the ground pad. Corrections for those require modeling, as discussed in the next section. It clearly is not so easy to measure this simple resistance!

$$\begin{pmatrix} V_1 \\ V_2 \end{pmatrix} = \begin{pmatrix} Z_1+Z_3+Z_4 & Z_3 \\ Z_3 & Z_2+Z_3+Z_4 \end{pmatrix} \begin{pmatrix} I_1 \\ I_2 \end{pmatrix}$$

$$\mathbb{Z} = \begin{pmatrix} Z_1+Z_4 & 0 \\ 0 & Z_2+Z_4 \end{pmatrix} + Z_3 \begin{pmatrix} 1 & 1 \\ 1 & 1 \end{pmatrix}$$

$$\therefore z_{11} = Z_1+Z_3+Z_4$$

$$\therefore z_{12} = z_{21} = Z_3$$

$$\therefore z_{22} = Z_2+Z_3+Z_4$$

Fig. 4 Z Parameter representation

To measure SVIA inductance, we can use the Z parameter representation (bottom of Fig. 3) to derive the equations in Fig. 4. The Z parameters are derived from the S parameters normally measured on our RF test system for this 2 port network, as in Pozar [2], table 5.2, reproduced for Z12 = Z21 in Eq. 1. Eq. 2 then gives substrate via inductance L from the imaginary part of Z_{12}.

$$\mathbf{Z_{12} = 2*Z_0*S_{12} / [\,(1-S_{11})*(1-S_{22}) - S_{12}*S_{21}\,]} \quad \mathbf{(1)}$$

$$\mathbf{Z_3 = R + j\omega L = Z_{12}} \quad \mathbf{(2)}$$

In the equations, Z_0 = 50 Ohms, $\omega \equiv 2\pi f$, and f = measurement frequency. This technique gives an inductance of about 15 pH for a 50 um diameter SVIA on the small structure in Fig. 3. An alternate series L-C resonant approach [3] has recently been used by Steen [4] and gives a comparable number for the same size SVIA, leading to some confidence that this number is reasonably accurate. However, further work on fully understanding this test and sources of stray inductance is ongoing, as discussed below.

MODELING

Our modeling efforts were aimed at understanding the DC resistance measurements. No electromagnetic simulations were attempted to predict inductance, though that has been attempted elsewhere [5].

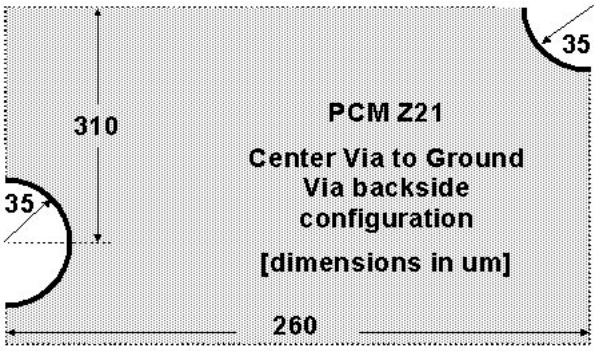

Fig. 5 ¼ of Backside metal return, structure of Fig. 2

We set out to be able to reasonably closely predict the measured resistance of the structure in Fig. 2, so that the SVIA resistance could be extracted from the measured values. Referring to Fig. 2, and assuming an electrical reference plane on the front surface, at DC we measure an SVIA to the back surface, with a return resistance to the 4 ground pads consisting of 4 parallel paths of back metal plus SVIA plus front metal connecting to the pad:

$$\mathbf{Rtotal = Rvia + 0.25 * \{ Rback + Rvia + Rfront\}} \quad (3)$$

where Rvia is the substrate via resistance R3. All of those are straightforward to model except for the backside metal component, shown in Fig. 5 (not to scale) for the large PCM structure.

An iterative, spreadsheet-based, finite difference - approach [6] was used to simulate the number of squares of this feature. A uniform square grid of 2.5 um was used for the calculation. Starting values of 0 and 1 V were put on the two SVIAs and the potential values in each cell were iterated to convergence. The resistance is taken from the potential difference between the two contacts.

PCM Structure	SVIA	SVia Diameter (um)	Measured Stucture R (mOhm)	Extracted R(SVIA) mOhm	L @ 1 GHz pH	L @ 10 GHz pH
Old	Tapered	50	9	4.5	10	9
New	Tapered	50	10	5.3	15	14
New #2	Wine Glass	35	13	8.5	28	26

Table 1. Typical Measured SVIA Test Structure Parameters and Extracted SVia Resistance, assuming a constant 21 mOhm offset resistance.

This was done for the various geometries used. This approach gives 1.71 and 1.77 resistance squares for the big and small structures, respectively. Our backside metal is normally 4 um of plated gold with a well-controlled sheet resistance of about 5.9 mOhm/sq.

After another SVIA to the front surface, the last piece of the resistance is a small length of frontside metal, amounting to 0.86 squares for either PCM structure. The frontside metal is a composite stack of interconnect metals with a sheet resistance of about 3.8 mOhm/sq. So, in general we measure

$$\mathbf{Rtotal = 1.25* Rvia + 0.25 * \{ 5.9 * \# Sq + 3.3 \}\ m\Omega} \quad (4)$$

which we solve for Rvia using the modeled number of squares for each PCM structure. Note the large influence of the backside metal sheet resistance and hence thickness, which needs to be well controlled for a stable measurement.

TEST RESULTS

Typical measured values for the various SVIA's commonly made are shown in Table 1. In the table, a constant offset of 21 mOhm was subtracted to compensate for cabling resistance, as mentioned above. Via diameter is as drawn. The different processes needed for different substrate types lead to some variance, but representative values are presented.

The very low resistance values are difficult to measure with our RF probes and HP 4145 parametric tester, which we see to have a resolution of 0.5 mOhm. Nevertheless, resistance is a well behaved measurement and is our primary means of monitoring our SVIA process. Most variation seen is attributed to plating thickness variations.

The extracted SVIA resistance following our model is also shown. The values for the old and new structures are close, but the old structure typically measures 1-2 mOhm lower. Both are higher than Rsv modeled as a simple cylinder of the average SVIA diameter unfolded into a rectangle, which gives about 3 mOhm.

Measured structure inductance shows some unexpected and as yet unexplained noisiness. The normal 10 – 15 pH value at 1 GHz is sporadically seen to jump up by 10 pH (e.g. see Fig. 7 below) without any accompanying symptomology in the resistance measurement. This can happen to a whole run or to a single wafer in a run, for any test structure, with a fresh calibration or not, and with new ACP's or old ones. Efforts to understand that continue.

We measure inductance from 0.1 to 14 GHz, and do typically see a slight decrease in L for higher frequencies, due to a structure stray inductance. This variation largely disappears if the differential slope of $\mathrm{Im}(Z_{12})$ vs ω is used instead of just dividing (see Eq. 2)

The increase in measured inductance from 10 to 15 pH for the same SVIA on the new structure compared to the old structure is also being investigated. As mentioned previously, 15 pH is more consistent with resonant test methods. The difference is thought to be from different parasitics for the new layout.

SCALING

Typically, the backside process needs to be optimized for a given SVIA diameter. We make diameters as low as 35 um, but 50 um is standard for many processes. In a given fab run, one can only vary SVIA diameters a relatively small amount. The results of one such set of tests are shown in Fig. 6, for a nominal 50 um SVIA diameter process, and show the expected increasing Rsvia with via size decreasing.

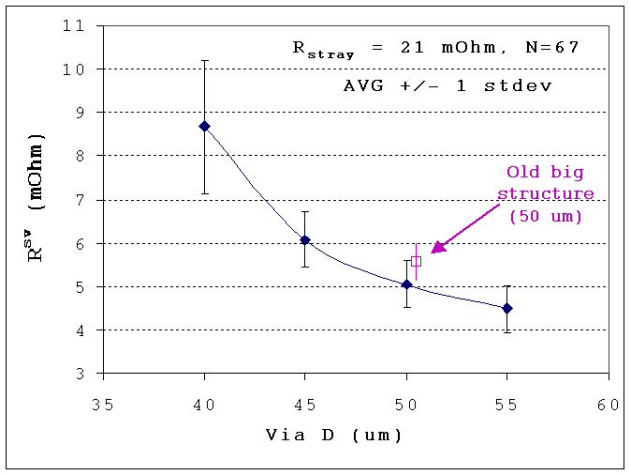

Fig. 6 Rsvia vs Diameter

Diameters as small as 40 came out fine, but smaller ones were not reliably opened with our etch process tuned for 50 um nominal vias. One can see the error bars increasing even for the 40 um size. The extracted SVIA resistance for the big PCM structure (50 um nominal SVIA diameter) is also shown, and was very close to the small structure resistance in this case.

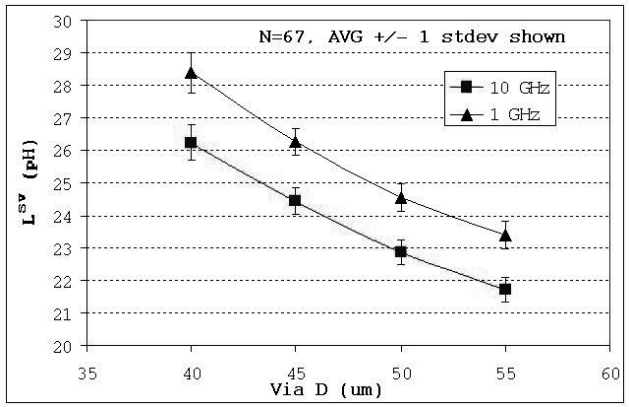

Fig. 7 Lsvia vs Diameter (with sporadic anomalously high L as mentioned in text)

Fig. 7 shows data for SVIA inductance at 1 and 10 GHz for the same experiment. One can see the previously mentioned frequency dependence, as well as one of our mysterious jumps up from 15 to 25 pH for this run. The same trend with diameter is seen in smaller experiments which did not have the anomalous increase. Inductance increases quite noticeably when via diameter decreases.

CONCLUSIONS

SVIA test is much more difficult than one would at first assume. Extreme care in measurement and interpretation is needed for all aspects. The resistance measurement is reasonably well controlled and understood, but inductance testing still has some unexplained noise. More work is needed to understand the details of that. A new smaller test structure is being developed, but still does not fully agree with the larger traditional structure.

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ACRONYMS

ACP: Air Coplanar (RF) Probe
PCM: Process Control Module
RF: Radio Frequency
SVIA: Substrate Via