

Failure Analysis and Process Improvements to a Through Wafer Via Process

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Abstract

GaAs devices in our factory employ through wafer via technology. Since the wafers are electrically tested prior to forming the via, construction must be robust. In an effort to reduce wafer costs, a die size reduction was required. During qualification and characterization of die shrink, the via process was investigated. The best method for testing the via is with a reliability test. A failure that was discovered in the via by the reliability test was a metal separation between the frontside and backside layers. This paper discusses the methods to eliminate metal separation in the via. The process improvements include optimized control of the GaAs etch; improved post-etch residue cleans and pre-metal deposition cleans; and increased thickness of the back side seed metal. Finally, new process controls and improved detection methods were used to verify via functionality. Our improved via passed all reliability tests.

INTRODUCTION

Factories are constantly being asked to drive costs down. One of the primary methods to decrease wafer cost is to increase the number of die per wafer. This can be accomplished by shrinking the die size. While much effort is put into how to shrink die for front side processing, the backside processing must also be explored. During characterization and reliability testing of a die shrink part, a failure was discovered related to backside processing. During reliability testing, a failure mechanism was discovered in the temperature, humidity, bias (THB) test. The initial indication of this issue came from two modules that were analyzed after failing electrically following 200 cycles of preconditioned temperature cycle stressing. Acoustic analysis revealed what appeared to be metal separation in the area of the power amplifier (PA) die on both units. Both of these failures could be traced back to a separation or delamination in the source via. Cross-sections of a via prepared by focused ion beam (FIB) showed the delamination, Figure 1. Upon this find, a team was formed to address the issue.

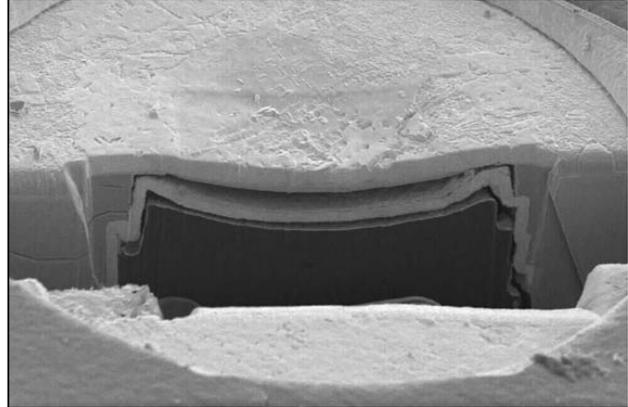


Figure 1: SEM image of metal delamination in via

The process sequence for constructing a through via at our factory begins with bonding a full thickness, fully processed wafer to a carrier. The carrier is used to support the wafer through the process steps. Processing of the composite begins with a mechanical and chemical thinning of the wafer. A photo pattern is then used to define the via openings. The GaAs is then etched using a plasma process, and the resist and etch residues are cleaned off. Metal is deposited on the wafer in two steps with a PVD sputter process for the seed metal followed by electroplating. The wafer is de-bonded from the support carrier and completes backend processing. Because of interactions within the process module, an analysis of any issue must begin by examining all process steps.

ANALYSIS OF PROBLEM

To begin, the location of the delamination is determined. In this case, it occurs between the frontside and backside metal along the seed metal interface. Based on our analysis, there were several possible causes for via delamination. The root cause related to via size decrease. The aspect ratio of the via was changed when the via was shrunk. The processes, in order, that change with aspect ratio begin with the plasma GaAs etch, specifically the overetch needed to clear smaller vias. This, in turn, affects the post-etch residues, which then affect the cleans needed to remove the residues. Cleanliness in the base of the via is key to providing a surface that the metal seed can adhere to. The increase in aspect ratio also makes metal step coverage more difficult for the seed deposition, which forms the adhesion layer between the front side and back side metal. In the analysis, it was obvious that all of these process changes

would provide a mode for delamination. Process improvements were needed in these steps to eliminate our issue.

PROCESS IMPROVEMENTS

One of the key concepts to understanding the via process module is that there is a high level of interaction between process steps. For instance, one of the first changes implemented in this project was an improvement to the thinning operation's measurement technique. An additional measurement point was added and another point had its location moved. In effect, these modifications tightened the within wafer thickness variation. In turn, this provides better process control of this step and a more consistent product for downstream processes. This change allows for process improvements in subsequent steps such as the through-wafer via etch. Also, this improved uniformity allows for easier dicing of final product.

With the reduction of within wafer variation, further optimization could be explored at the through-wafer via etch process. The through-wafer plasma etch process utilizes an inductively coupled plasma (ICP) with a BCl_3/Cl_2 chemistry. During the GaAs etch of the through-wafer via, under-etching (NEO), as well as over-etching, can occur. A strong interaction exists between the percent over-etch and the amount and types of residues formed. Extended over-etch creates thicker veils.

Thus, an important parameter that impacts this veil formation is the incoming thickness uniformity as discussed previously. Differences in thickness across the wafer will require longer over-etch to ensure all vias are etched to the front-side metal. The more uniform the wafer thickness, the closer in depth are each of the through-wafer vias, allowing for all vias to clear to metal at a similar time, also minimizing the veil formation. With via depth differences minimized, an optical end-point system (OES) was evaluated. An end-point system was installed and an algorithm was developed to look at the gallium emission, (Figure 2). A robust endpoint algorithm was implemented which resulted in an improved control etch and thus a consistent etch residue. Developing a consistent etch residue or veil makes the subsequent process step, veil removal, easier and repeatable.

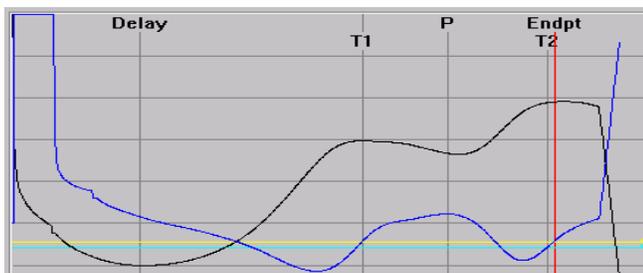


Figure 2: Example of an end-point trace

The veil that is formed during plasma via etch is very complex. Because the plasma etch uses a photoresist mask

to etch through GaAs, stopping on a gold layer, the veil consists of by-products from all materials. From previous work¹, the veil material consists of a gold-rich layer, and a carbon-rich layer which is intertwined with gallium and arsenic by-products (Figure 3). Though previous work had developed a sequence of cleans steps based on this layered theory, some optimization still needed to be completed to make it more robust for via shrink.

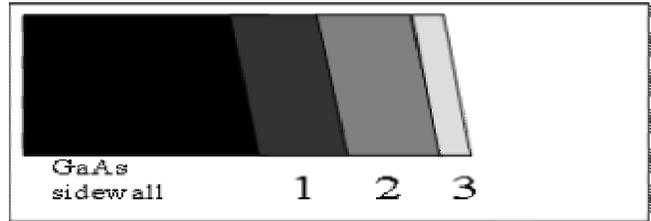


Figure 3: Depiction of the veil layers

The main theme through the veil cleans improvements was to improve flow of wet chemistry to vias. The transport of chemical becomes even more critical as the aspect ratio increases. The first problem noted in this module was the use of an aspirated Spray Acid Tool (SAT) for the first step in the module, the gold veil etchant. The gold-etchant should completely wet the entire via including completing a subtle and consistent etch of the catch-pad. From optical inspections, roughness of the gold on the catch-pad was not consistent, proving that the via was not completely wetting (Figure 4). Process improvement efforts determined that cleaning vias with an aspirated chemical was not desirable, but that a pumped delivery with reduced revolutions per minute (RPM) provided a good solution. Utilizing several iterations, pumped flow could force chemical in the via and remove veils. The difference in these two processes can be seen in Figure 4.

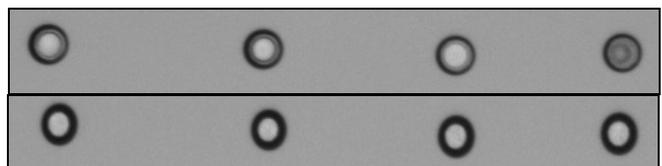


Figure 4: Aspirated process (top), Pumped process (bottom)

The next step in the process requiring further review was the photoresist and carbonaceous veil removal. This process step utilized a spray solvent tool (SST) with a GenSolve¹ solvent chemistry. To improve wetting with this particular chemistry and the wafer surface, RPM was increased.

The final step investigated serves a three-fold purpose: final veil removal, via wall smoothing, and backmetal preparation. First to improve the manufacturability, the number of iterations was reduced from eight to one. To reduce the across-wafer uniformity and improve the chemical and resonance time within the via, RPM was decreased as well as time increased. Both optical

inspections and SEM images were used to ensure improvements to via cleanliness, as well as keeping the same level of via side-wall smoothing.³ To ensure that the backmetal adhesion was not compromised, the break and slide method of backmetal adhesion testing was performed².

One of the issues with this type of process improvement is the attempt to discern whether modifications to the process truly improved via cleanliness. Original studies utilized manual optical inspections and sample counts of vias, but to account for subtle differences between processes modifications, a better system needed to be developed. To better quantify any changes made to the process, an automated backside-via inspection was developed to inspect vias prior to, and after, the cleans module³. The methodology that is used to inspect the through-wafer vias greatly assisted with development work. It was utilized in optimization of all steps in this process module. It also addressed long-term concerns, including the detection of any possible inline excursions. An optimized via cleans process ensured that the through-wafer via was free of veils and provides a clean surface for the sputtered seed layer.

While work was on-going to improve cleans, the metal adhesion layer was also under investigation. Because the source of delamination was at the base of the via, originating from a very thin layer, high magnification TEM cross-sections were used for the investigation. The TEM images showed an accurate thickness of the metal between the gold layers, and it also showed an interface on one side of the Ti layer (Figure 5-7).

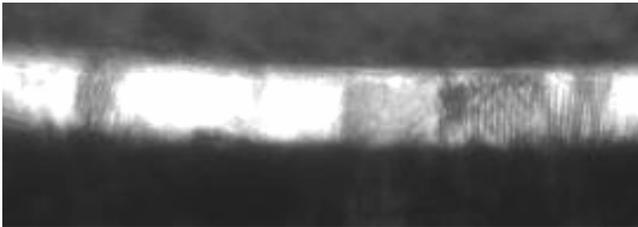


Figure 5: TEM image of adhesion layer thickness before change (160Å)

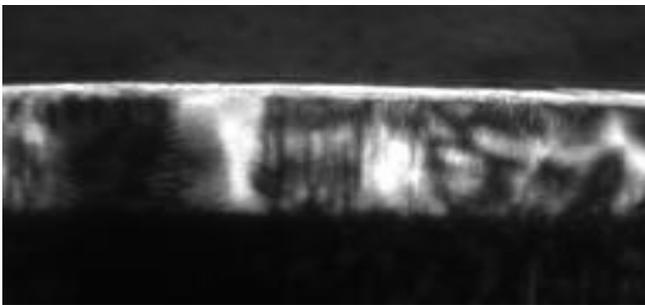


Figure 6: TEM image of adhesion layer thickness after change (320Å), note the interface layer (30Å)

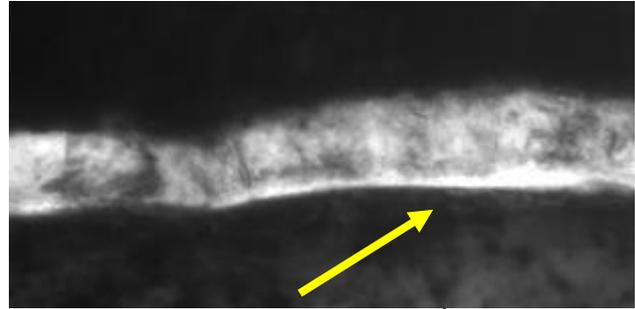


Figure 7: TEM image showing interface layer (50Å)

Based on internal materials experts' opinion, this layer needed to reach a critical minimum thickness to create an effective adhesion layer. This minimum thickness was on the order of 200Å. The interface layer was also thought to be a possible source of reduced adhesion and needed to be understood. When via size was reduced, aspect ratio increased, thereby making metal step-coverage more difficult. To account for the change in aspect ratio, the thickness of the metal layer was increased. The increased thickness also provided process marginality for coverage in vias to compensate for surface roughness or veil material that was not removed by the cleans (Figure 8). The metal was able to create an effective adhesion layer over surface texture or on top of veils and help prevent the via from having a source for delamination. The interface layer was investigated and related to the time delay between the clean and seed metal deposition. In keeping the existing system in place to minimize the time between processes, the interface did not prove to be an issue.

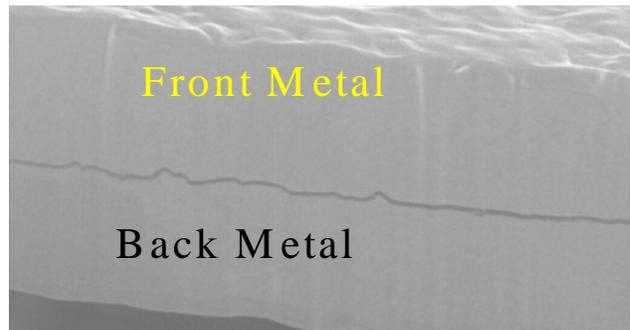


Figure 8: SEM cross section showing the surface texture of the layers

Following improvements to etch, cleans, and metallization processes described in previous sections, via cross-sections indicated that the source of spectacular failures had been eliminated. This was also confirmed by electrical and physical reliability testing.

However, during the physical (polishing) preparation of samples for in-line monitoring, a weakness in adhesion was discovered. This discovery indicated a small percentage of vias still had some delamination present at their base between the front-side Au and the back-side Ti layers (Figure 9).

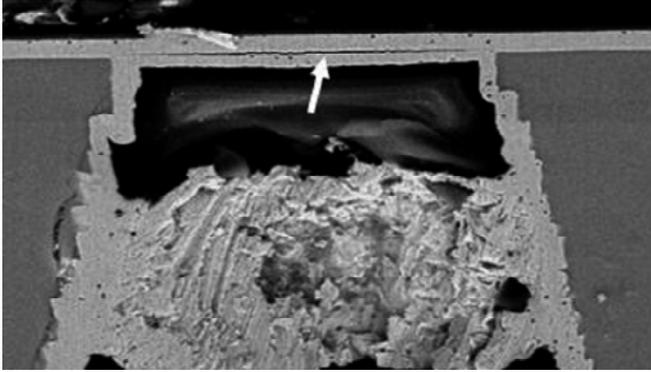


Figure 9: SEM view of via cross-section. Arrow indicates separation between front- and back-side metal.

Further experimentation using in-line quality SEMs (QTSEM) resulted in the discovery of an interaction between two processes which could create further adhesion issues. The processes in question were the pre-deposition wet clean and RF etch that occurs in situ, prior to seed metallization. Neither process step would have been an issue if the other would have been kept at a nominal level, but the combination at minimum levels compromised adhesion between the metal layers. Repeated experiments confirmed that either, but not both could be run at any level without these adhesion failures. The team made a small adjustment to the wet clean to provide robust adhesion to the front-side and back-side metal (Figure 10) and will continue work to optimize the module as part of a continuous improvement program (CIP).

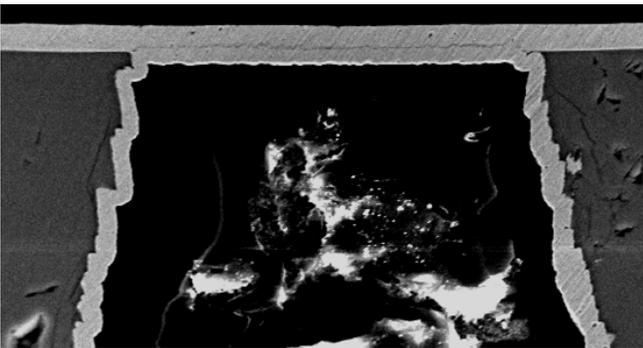


Figure 10: SEM view of via cross-section of sufficient adhesion between front- and back-side metal.

CONTROLS

Reliability studies are critical in stressing the via and provided the initial data indicating the delamination issues. Based on this experience, reliability tests are a requirement for process changes within the via module. Due to time constraints in constantly performing reliability studies, some form of in-line monitoring must be performed to avert issues. Because prior in-line controls were inadequate at detecting this problem, it was determined that better process

controls were needed. The new controls included: SEM imaging of via cross-sections on a sample of the wafers produced, looking for delamination, adhesion layer thickness monitoring using TEM images on a sample of wafers, and automated backside via inspections prior to metallization to verify functionality of cleans. These, in conjunction with reliability tests, provide a robust system for via functionality.

CONCLUSION

Key process changes were made to eliminate metal delamination and build a robust through-wafer via. These include plasma etching of the GaAs with endpoint control and consistent over-etch; optimized cleaning processes for post etch veil removal; improved clean prior to metal deposition; and an increase in the sputtered seed deposition. Parts were assembled and sent for reliability testing using the improved process. There were no failures in three groups of studies. Based on these results, the new process was implemented, with more extensive reliability studies done in the future with larger sample sizes. In line controls were also implemented to maintain the process and provide additional qualification methods for future process improvements.

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