LED Technology Trends

D. Eissler, **S. Illek, G. Bogner**

OSRAM Opto Semiconductors, Leibnizstr. 4, D- 93055 Regensburg
Dieter.Eissler@osram-os.com, phone; ++49 941 850 1592

Key words: LED technology trends, light extraction, miniaturisation of LED, LED power application, Thin Film technology.

Abstract
We will describe trends in the LED market and the consequences on the technical roadmap of LED-products. This will prescribe the focal points and direction of the upcoming manufacturing technologies. Two main trends are reinforcing at the moment. The first is an ongoing miniaturisation; the second one is the increasing number of power applications coming up due to higher chip efficiencies.

INTRODUCTION
An ongoing first trend is the miniaturisation of LED chips down to 150µm in square and 100µm in chip thickness, fitting for mass production. Complete micro devices are only 1000x500µm in square. The driver for this development is the limited space in applications as mobile communication and the lowest capital cost possible for the manufacturing processes. Also the LED material itself is still expensive mainly due to substrate costs and epitaxy (Fig.1).

The second direction of the trend is increasing the light flux for: power LED light sources, projection systems and exterior car LED solutions, including the head lamp where we really can gain new markets for our products.

But it is even more important, that the today power LED light sources are the first step for a wide scope of general illumination with LED in the future [1], [7], [8], (Fig 1).

These beforehand mentioned trends to miniaturisation and high flux are determining the marketing and technological roadmap and accordingly the resulting manufacturing technology. A particular requirement for both, power and miniature applications is the improvement of the efficiency of the chips and the complete application (Fig 2).

In the following paragraphs we will discuss the influence of this two trends miniaturisation and power applications on the technology roadmaps of: substrates/epitaxy, chip processes and the end of line/application technologies.

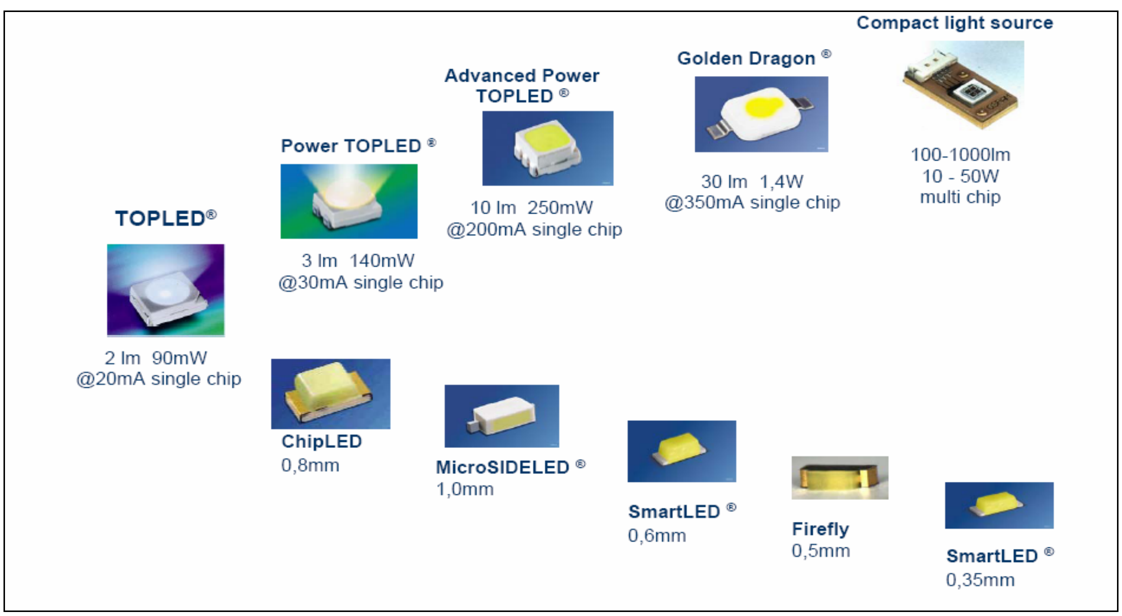

Fig.1: Development of LED technology from a standard LED in direction of micro and power application

SUBSTRATES, EPITAXY OF CHIPS

Consequences for the manufacturing technology to improve the internal efficiency are therefore: a continuous development of the epitaxy MOCVD equipment and the process itself, to be as cost effective as possible. Furthermore it is important to go on with local defect reduction even on high efficient LED structures due to continuous improvement of the substrates and the epitaxy process [2], [3].

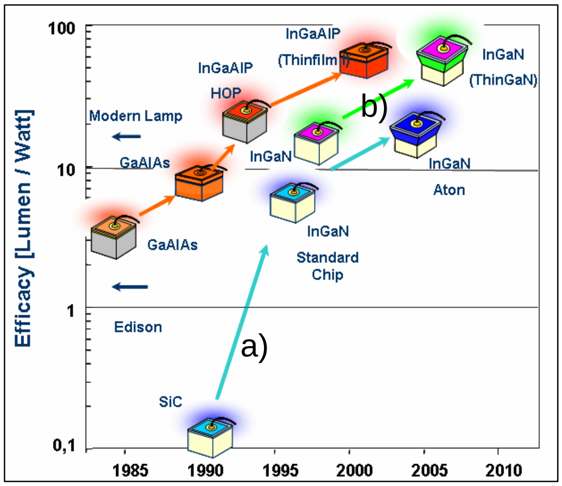

Fig. 2: Efficacy evolution of InGaAlP and InGaN LED-chips in the last decade, a) InGaN blue, b) InGaN green

Most effective for high efficacy blue diodes (Fig 2), especially for blue lasers, is the use of homo substrates, i.e. GaN bulk material. This brittle, 1 inch diameter crystals, are a challenge for manufacturing technology [3]. Standard substrates (SiC, Sapphire, and GaAs) should be compatible with the 4" technique in order to minimize fabrication costs in the next years. Therefore the focus of interest for the manufacturing technology is to reduce wafer breakage and preliminary defects as scratches, and intrinsic grown particles. Naturally these facts are more pressing for large power chips [2].

The precision of mechanical processes as wafer grinding, dicing, advanced handling as well as other mechanic preparation methods will be much more important in the future for all the products. At first they influence directly the height of our miniature products and the chip yield due to less cracks and chipping. Secondly, because the thinnest substrates possible take us to less power consumption, it will reduce the heat resistance to a minimum, as well as the electrical resistance, in the case when a conducting substrate is used.

CHIP TECHNOLOGY

OSRAM thin film LED technology (Fig 3), is a significant step forward to achieve the goal of high external efficiency and scalability from micro chips up to huge, high current power chips (Fig 4), [4], [8].
An other possible approach is the inverted truncated pyramid [5], where the absorbing GaAs substrate is replaced with a GaP window by direct wafer bonding techniques after the epitaxial growth.
Further obvious realisation of modern LED is a classical flip chip concept. This can be carried out successfully especially for transparent substrates as sapphire.

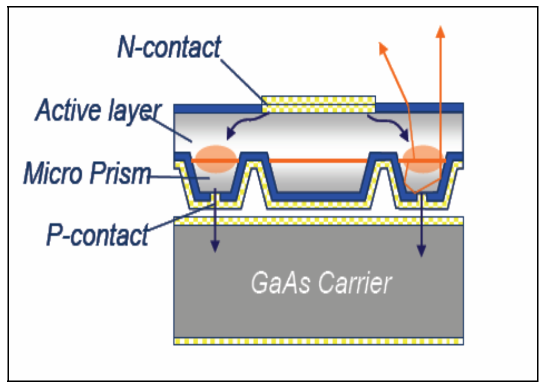

Fig. 3: Schematic view of a Thin Film LED

A successful implementation of the thin film technology is based on the establishment of a number of new processes in a production environment.
Crucial is the creation of buried micro reflectors or at least a surface roughening in the LED structure. These micro reflectors were dry- or wet etched and break the internal wave guide effect in the diode structure for emission angles larger than the critical angle of total reflection (Fig. 3). With buried micro reflectors the light can be emitted by a few reflections without evident reabsorption in the active layer [4]. A main advantage of this concept, compared to the classical flip chip or the inverted truncated pyramid is: the mainly forwarded light which leads to a lambertian emitter and a simple scalability from a small die up to big chips for high current applications. Even blue InGaN chips [9] and longer wavelength InGaAlP [4] and AlGaAs chips can be fabricated nearly in the same way and manner.
For the production technology the thin film concept needs a very precise control of etch solutions, as well as control of etch depths. In general we need material sensitive etch stops throughout all the many different chip layers.
The structures itself are relatively large, in the range of some tenth of microns (Fig. 4). So the photo technique in the future manufacturing will be conventional mask aligning. The resolution is sufficient for all the possible cases. May be, for photonic crystals, where we need sub

micron structures, stepper technique must be used. The overlay precision from layer to layer is the critical parameter in the photo technique, simply to get the smallest chip possible. There are several reasons for this: 3-8 photo layers are necessary for a modern chip (Fig. 4), structured front- and backside contacts are used. With high overlay precision it is possible to have smaller tolerances from layer to layer, so it is possible to save the expensive LED material, this is especially true for the smallest chips.

A second important production technology class are the different bonding technologies.
At first the direct wafer bonding, in combination with a DBR (Distributed Bragg Reflector) needed e.g. for truncated inverted pyramids [5], is a possibility to make a high efficient LED. This van der Waals force supported technique is based on: atomically flat surfaces, extremely clean and particle free environments, to work with high yield. Especially for large chips, high effort is needed in production to get good yields [6].
For the flip chip variants and also conventional high current chips soldering bumps or eutectic solder layers have to be implemented with all the difficulties well known from galvanic steps or other thick film metal deposition techniques as particle generation or chemical residuals.

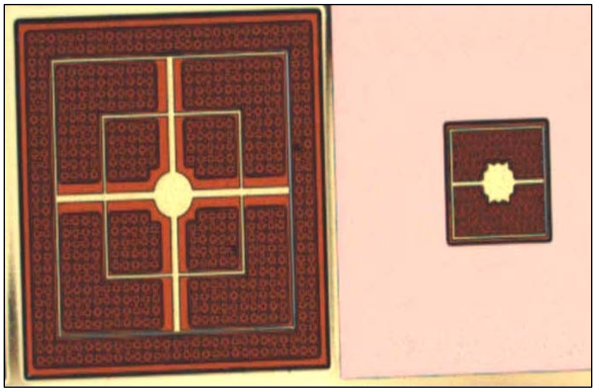

Figure 4: Top view on a 1mm thin film chip and a 300µm chip directly near by each other on the same wafer (buried micro reflector). This demonstrates the scalability of our Thin Film technology.

For thin film technology wafer scale soldering technologies are a core competence. Wafer scale soldering enables the benefit of removing the absorbing substrate as well as direct and undisturbed front emission (Fig. 3) [4]. For the Thin Film LED production technique, at the front side of the wafer, on top of the buried micro reflectors a contact is deposited. On top of this contact the eutectic bond is formed together with a carrier wafer. The backside substrate can be removed now, so we get the upside down eutectic bonded thin film diode. This technique needs deep knowledge of metallurgy and barrier physics. On the other hand we get a very reliable, low resistance, scalable bond [4], [7]. This technique is useful especially for high flux LED (Fig. 5).

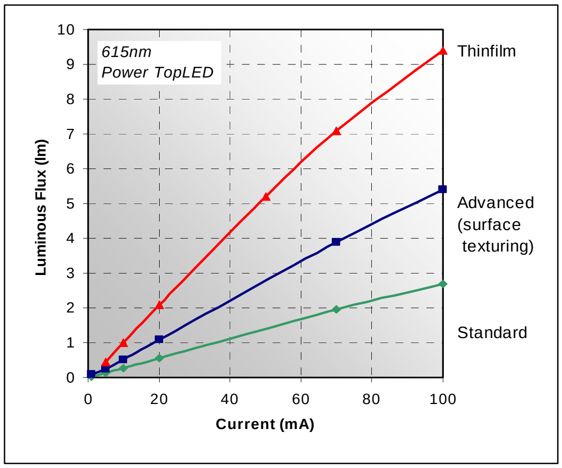

Figure 5: The influence of new technologies as surface texturing and Thin Film technology (615nm) with buried micro reflectors on the luminous Flux of a LED.

END OF LINE, APPLICATION

The challenge in the end of line technology, especially the testing will be to identify the scrap on the lowest added value possible. The best solution is to drop the scrap direct after epitaxy, or in the early process steps of the front end. The testing area will be supported by advanced machine and process control, combined with classical electrical data management as seen in the silicon world.
Additionally the testing field will be focused to ongoing cost reduction. Better yields and more process stability in the front end generate space for omitting classical testing steps.
The die bonding will handle smaller chips, now we have 150µm chip size in square in production. The chips for micro devices in future will be not much bigger as the usual bond pads of a today standard chip. To handle such small dies without slowing down the cycle time of die bonders and additionally without losing reliability and precision is a big challenge.

Chip soldering technologies will dominate more and more the field of power chips, due to better thermal coupling to the substrate.
For power applications a high internal and external efficiency will help to minimize the heat creation and optimize the heat dissipation of the system. This is well known from high power IR lasers. Complicated material mixes will be needed as ceramic and metal core boards. Interaction of the entire LED application with LED package and chip itself is becoming more and more important for advanced applications.

For systems such as multi chip modules heat dissipation plays an important role as well. Precision assembly of multi chip modules will move forward the advanced packaging technology and enable freedom for new designs.
In general this means that LED power applications appeal in terms of used manufacturing technology, as well as complexity, more and more to the MEMS and MOEMS applications.

CONCLUSIONS

We showed that due to the splitting of the main market in micro devices for mobile communication and on the other hand in power devices e.g. for exterior car applications, projections and LCD backlighting we get a splitting of the LED market and technology.

The first part includes very small, size-critical chips and devices.
The second part represents large power devices with real light engines inside. These light engines are the core of the future vision of room illumination by LED [1], [8].

Jointly for both technologies we need the highest efficacy of the integrated application and the lowest cost of a Lumen of light. The micro devices need very small dimensions of chips. The power devices are extremely heat critical; we have to avoid non radiative recombination due to heat losses.

For the production technology and cost position this leads to the demand of scalability of the chips. In the case of wide scalability of a chip technology it is possible to deliver many different devices and applications with technologically nearly identical chips.

High efficacy can be reached with thin film technologies, and other approaches e.g. [5]. We showed the fit of our Thin-Film technology for reliable mass production. Key technologies are for example:

- Mechanical processes as grinding and advanced handling for thinner, high yield devices.
- Bonding processes for avoiding absorbing substrates and the creation of lambertian emitters.
- Advanced handling of very small chips. In the backend and applications technology we will handle chips smaller as 150µm in square in production.

The applications were dominated by a multi material mix of heat sinks and optics. An integrated (theoretical, numerical) approach of chip, package and application is necessary to be technologically successful in future.

ACKNOLEDGEMENT

For fruitful discussions and material we acknowledge our colleagues: V. Haerle, A. Ploessl, P. Stark, N. Stath, K. Streubel, H. Zull.

REFERENCES

[1] *R. Haitz, F. Kish, J. Tsao, J. Nelson, 1999 Optoelectronic Industry Development Association, Washington DC, October 6. 1999*

[2] *R. Stevenson, Compound Semicond. Vol.**10**/10, p. 18-22 (Nov. 2004)*

[3] *K. Evans, Compound Semicond. Vol.1**10**/9, p. 27-31 (October 2004)*

[4] *S. Illek, I. Piezonka, A. Ploessl, P. Strauss, W. Wegleiter, R. Windisch, R. Wirth, H. Zull and K. Streubel., Proc. SPIE, Vol. **4996**, 2003, p.p. 18-25*

[5] *M.R. Kramers et al., Applied Physics Letters, **75** [16], pp. 2365, 1999*

[6] *A. Ploessl, G. Kraeuter, Mat. Sci. Eng., **R 25**, 1999, p.p. 1-88*

[7] *T. Withaker, R. Stevenson, Compound Semicond. Vol.**10**/11, p. 18-19 (Nov. 2004)*

[8] *M. Hatcher, Compound Semicond. Vol.**10**/11, p. 25, 26 (Nov. 2004)*

[9] *V. Haerle; B Hahn; J. Baur; M. Fehrer, A. Weimar; S. Kaiser; Eisert; F. Eberhard; A. Plossl; S. Bader, Proc. SPIE , 2004, Vol.**5187**, p.34-40*

ACRONYMS:

LED: Light Emitting Diode
MOCVD: Metal Organic Chemical Vapour Deposition
MEMS: Micro Electro Mechanical System
MOEMS: Micro Opto Electro Mechanical System