Oxygen Plasma Damage Study on InGaP/GaAs HBTs

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Abstract

This paper presents the results of investigations into the effect of oxygen plasma damage to InGaP/GaAs HBTs. The study examined the PCM data and the results of reliability tests performed on devices that had been exposed to various plasma intensities at two different processing steps. Our results show that direct exposure of the HBT to plasma after formation of the base pedestal can result in poor reliability. The degradation in reliability had an unusual correlation to plasma intensity. In addition, a thin SiN layer can effectively protect the HBT from plasma damage.

INTRODUCTION

Plasma processes are used extensively in the fabrication of GaAs HBT's for etching, cleaning, stripping photo resist and depositing thin films. Although most modern plasma systems are designed to minimize plasma damage to the HBTs, it is still an area of concern in the development of manufacturing processes. The plasma damage threshold of FETs and HEMT type devices has been well documented [1,2]. Less well known, however, are the effects of plasma damage on HBTs at the critical early steps in the formation of transistors [3-7]. Because dry etching and resist removal have begun to dominate manufacturing methods in the early stages of processing, it is important to know what effects to look for in qualifying these processes and how to minimize these effects.

EXPERIMENTAL METHODS

The experiments were performed on InGaP/GaAs HBTs built on a standard double mesa design. Plasma damage was introduced by processing the HBT wafers in a Unaxis Versalock 700 ICP etch system using an oxygen plasma. A schematic of an ICP system is shown in figure 1. The design of the Versalock system allows for good control of the plasma DC bias voltage through proper application of the applied RIE power. In this experiment, the ICP power was held constant at 600 watts while the RIE power was varied from 0 to 400 watts as needed to produce the desired DC bias voltage. Bias voltage is used as the measurement gauge because it has more direct meaning than power, the effects of which will vary depending on the equipment design. The correlation between bias voltage and RIE power was found to be 98%.

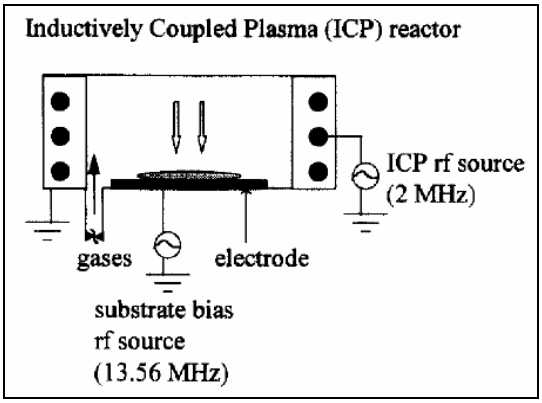

Figure 1: ICP etch system showing both RIE and ICP power source.

To test the sensitivity of the transistor to plasma damage, the experiment was carried out at two different steps in the process. The first phase of the experiment was carried out after the deposition of a thin SiN film and the formation of the base contact. A similar point of processing is shown in figure 2. In this case only a small portion of the ledge, near the base contact, was directly exposed to plasma whereas the rest of the wafer was covered by nitride.

In the second phase of the experiment, wafers were exposed to the plasma immediately after the formation of the base pedestal and before the emitter ledge was protected by the nitride. In this case both the emitter ledge and sidewalls of the emitter mesa and base pedestal (BP) mesa were exposed. As this gave the most interesting data, the experiment was conducted on two different lots about two

months apart. The targets for plasma DC bias were different between the lots but overlapped somewhat in order to confirm the data. Control wafers which were not exposed to plasma were included in each experiment.

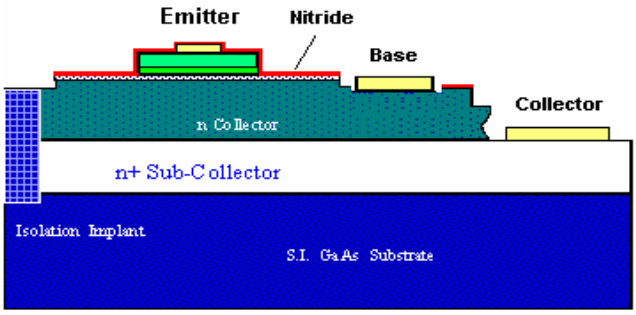

Figure 2: HBT transistor showing thin nitride film and base contact.

At the completion of processing, standard DC and RF parametric tests were carried out prior to reliability testing. The reliability test was performed on HBT transistors with emitter areas of 56μm^2 using custom built reliability test systems at Skyworks. The transistors were subjected to high temperature and high current stress. The stress conditions were 25KA/cm^2 emitter current density and 200^{o}C case temperature (~305^{o}C junction temperature). The electrical/thermal stress was interrupted periodically to allow device characterization to be performed at room temperature. The HBTs were characterized by forward Gummel measurements and base-emitter/base-collector diode I-V measurements using a semiconductor parameter analyzer. A 50% DC current gain (beta) decrease was used as the device failure criterion. Sixteen devices were measured for each wafer variants and their average stress lifetime is calculated and referred to as t50%.

RESULTS

Wafers that were exposed to the plasma after the formation of the base contact, with the ledge mostly protected by nitride, showed no adverse effects in either parametric data or reliability. For the two lots processed (at different times) with the ledge exposed to plasma, most DC parametric data showed no correlation to the bias voltage used in the experiment. One notable exception was the base-collector diode breakdown voltage (BVcbo) which is shown in figure 3. The BVcbo shows an inverse relationship to the plasma intensity. In addition, the emitter sheet resistance was found to increase with increasing plasma damage. This relationship is shown in figure 4. For these two figures, the data for one lot is plotted using dots while the data for the second lot is plotted using rectangles.

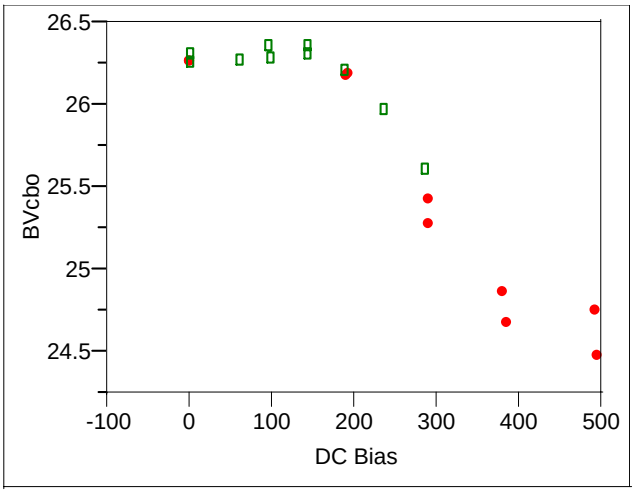

Figure 3: DC Bias plotted against the collector-base breakdown voltage.

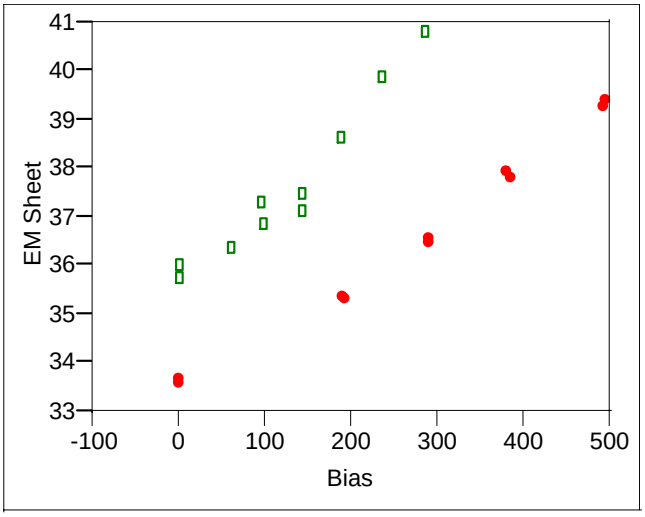

Figure 4: Bias voltage of the plasma plotted against emitter sheet resistance.

The surprising data was found when the results of the reliability testing were analyzed. The reliability data show a double cusp when plotted as t50% versus the plasma bias voltage as shown in figure 5. Control wafers that were not exposed to plasma (0V bias) exhibited a reliability t50% of approximately 1000 hours. T50% degrades rapidly with exposure to increasing plasma densities to about 100V. A wafer exposed to even a small (2V) bias shows a steep drop in t50% to about 250 hours. The stress lifetime of the devices then increases as the bias voltage approaches 300V before finally degrading again.

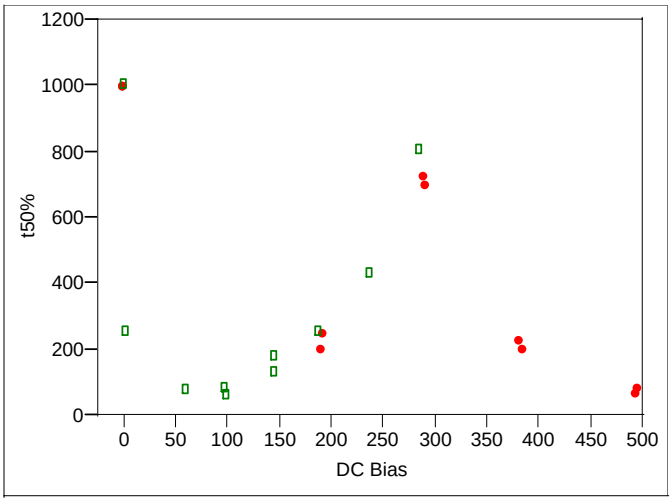

Figure 5: Bias voltage versus t50% including control wafers that were not exposed to plasma damage. The data overlap between the two lots processed two months apart confirms the cusp in the data.

DISCUSSION

F. Ren et al. [5] have reported that argon ICP plasmas cause no damage to AlGaAs/GaAs HBTs. No drop of current gain was observed by them for ICP, where as with RIE, even at bias voltages below 30 V, damage occurred, manifested by loss of current gain. They concluded that in order to get high etch rates, more ICP power must be added in etch systems capable of both modes, in order to keep the RIE bias low. C.H. Hsu et al.[7] have reported similar results with nitrogen as well as argon plasmas (nitrogen plasmas being relevant to deposition of SiN passivation).

Dry etch damage is caused by bombardment of a surface by ions. At biases in the range of 100V, atomic oxygen ions are stopped within a few monolayers of the surface. Molecular ions should penetrate even less. A small fraction of the ions channel, causing deeper penetration. High density plasmas may have more atomic ions present and may penetrate more. If an amorphous nitride passivation layer is present, the effect of channeling may be completely eliminated. This seems to be the case in our experiment with the HBT covered by the SiN layer after base pedestal formation.

M.Rahman et al. [6] have studied dry etch damage in III-V semiconductors, by using non-invasive methods, like photoluminescence (PL) from multiple quantum well structures, to detect depth of damage. They have verified that extent of damage (N_D), as measured by loss of PL, drops exponentially with depth. $N_D(y) \sim Ji \exp(-y/\lambda)$, where Ji is the ion flux, λ is a characteristic length and y is the depth.

If the ion damage occurs primarily from the top of the surface, it should drop exponentially with depth. As etch bias increases, damage should increase and the device reliability should become worse. Surprisingly, in our experiments with InGaP/GaAs HBTs, we do not see exponential or linear correlation between the plasma bias voltage and reliability stress lifetime. Instead, $t_{50\%}$ drops at low bias voltage (below 100V) and increases at the peak around 300V bias, before falling again at higher plasma bias voltages. From our PCM data, the correlation between the DC current gain beta and the plasma bias voltage is not conclusive as one lot has good correlation whereas the other one doesn't. The beta change was also small and within normal process variation.

The correlation between PCM base collector diode breakdown voltage and plasma bias voltage indicates damage to the base pedestal side wall. Degradation of base-collector breakdown voltage was also reported by Lee et al. [4]. The increase in emitter sheet resistance with plasma damage also indicates damage to the emitter mesa, and also likely to the side wall as the emitter effective resistance (Ree) did not change. This is plausible as both emitter mesa and base pedestal mesa, in addition to the InGaP ledge, were exposed to the plasma, as depicted in figure 6. The base layer, on the other hand, is protected by the InGaP layer and therefore the base sheet resistance was not affected.

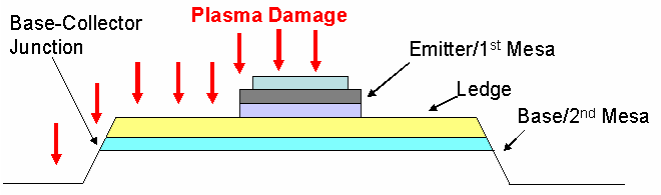

Figure 6: Plasma exposure pattern to emitter and base.

As the emitter mesa and BP mesa damage may contribute to the long term device reliability degradation, further experimentation and characterization are needed to decouple the damage from ledge, from emitter mesa, and from BP mesa side wall in order to fully understand the plasma damage mechanism. This may help to explain why the device reliability stress lifetime doesn't correlate with the plasma damage as theoretically expected.

CONCLUSIONS

In summary, we have investigated the effects of exposing HBTs to plasma damage at two different processing steps. The results show that HBTs exposed to plasma after BP formation without nitride protection sustain damage to the emitter mesa and BP mesa sidewalls. The device reliability is also severely degraded, however, it is not

linearly or exponentially correlated with plasma damage bias voltage.

Further experimentation is needed to fully understand the plasma damage mechanisms in our experiment and their impact on the device long term reliability.

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REFERENCES

[1] M. Tong et al., *A comparison study of wet and dry selective etching of GaAs/AlGaAs MODFETs*, J. Electonic Mater., vol 21,9, (1992)

[2] V. Kumar et.al., *Effect pf oxygen plasma on the electrical characteristics of GaAs MESFETs*, Solid State Electronics, **44** (3), (2000)

[3] William Liu, Handbook of Heterojunction Bipolar transistors, John Wiley & Sons (1998)

[4] J.W. Lee et. al., *Comparison of dry etch damage in GaAs/AlGaAs HBTs exposed to ECR and ICP Ar Plasmas*, Solid State Electronics, vol 42,733 (1998)

[5] F. Ren et al., *Dry Etch damage in ICP exposed HBTs* , Appl. Phys. Lett., vol 70, 2410 (1997)

[6] M. Rahman et al. *Studies of damage in low-power reactive-ion etching of III-V semiconductors*, J. Appl. Phys., vol 89, 2096, (2001)

[7] C.H. Hsu et al. , *Effect of N2 and Ar plasma exposure on GaAs/AlGaAs HBTs*, Solid state Electronics, vol 45, 275, (1997)

ACRONYMS

HBT: Heterojunction Bipolar Transistor
SiN: Silicon Nitride
ICP: Inductively coupled plasma
RIE: Reactive Ion Etching
PL: Photo luminescence
BC: Base collector
BP: Base pedestal
PCM: Process control monitor