Shallow Mesa Isolation of AlSb/InAs HEMT with AlGaSb Buffer Layer Using Inductively Coupled Plasma Etching

P. Nam, R. Tsai, M. Lange, W. Deal, J. Lee, C. Namba, P. Liu, R. Grundbacher, J. Wang, M. Barsky, A. Gutierrez-Aitken and S. Olson

Northrop Grumman Space Technology, Microelectronic Product Center,
Redondo Beach, CA 90278
Tel: (310) 813-8820, Fax: (310) 812-9501, Email: peter.nam@ngc.com

Key word: AlSb/InAs HEMT, AlGaSb buffer, mesa isolation, ICP etching

ABSTRACT

A mesa isolation process of AlSb/InAs HEMT has been developed by using inductively coupled plasma etching. The etch rate is well controlled and the resulting mesa floor demonstrates a significant improvement in smoothness as compared to a wet-etched floor. Devices fabricated by this technique show a revolutionary RF performance of f_T =220 GHz and f_{max} = 275 GHz at 170 mW/mm for a 0.1-µm gate.

Introduction

The InAs-channel HEMT has the potential to enable low-noise, low-power, and high-speed circuits utilizing superior electron mobility and velocity in InAs compared to those of the InGaAs-channel HEMT. As shown in Table 1, key electronic material properties of InAs are superior to those of InGaAs and GaAs. Unfortunately, there is no lattice-matched 6.1 Å semi-insulating substrate. Metamorphic growth on GaAs substrates using the $Al_xGa_{1-x}Sb_yAs_{1-y}$/InAs material system has proven to be a viable alternative for state of the art AlSb/InAs HEMTs [1-2]. This buffer layer effectively buries the dislocations. However, many of these AlSb/InAs HEMTs had employed a relaxed AlSb buffer that is highly reactive in air. Thus, outside the active device region, this AlSb buffer needed to be etched away by deep mesa etching. However, the non-planar topology after deep mesa etching makes it difficult to integrate a device with MMIC components such as capacitors, resistors, and inductors.

Previous studies reported that $Al_{0.7}Ga_{0.3}Sb$ insertion on top of an AlSb layer enables a shallow-mesa isolation stopped at $Al_{0.7}Ga_{0.3}Sb$ [3]. This shallow-mesa isolation was performed by a wet etch based on an acetic and hydrofluoric acid solution. However, wet etching is more labor intensive and can be less repeatable in mesa isolation steps. It is imperative to develop a dry-etching technology for a more controlled and less labor intensive production process.

In this paper, we report a shallow-mesa isolation etch of AlSb/InAs HEMTs using inductively-coupled plasma etching with Cl_2-based chemistries.

Table 1. HEMT channel Electronic Material Properties

Property	InAs	$In_{0.53}Ga_{0.47}As$	GaAs
m_e^*	0.023	0.041	0.067
µ (cm^2/V-sec)	20000	8000	4500
Peak Velocity (10^7 cm/sec)	4.0	2.7	2.2
Γ-L valley separation (eV)	0.9	0.55	0.31
Band Gap (eV)	0.36	0.72	1.42

Device Structure and Manufacturing Technology

Figure 1 shows a baseline AlSb/InAs HEMT epitaxial structures grown by molecular beam epitaxy (MBE) on semi-insulating 3” GaAs substrates at NGST. On top of a 2.0 µm AlSb buffer layer, a 0.3 µm $Al_{0.7}Ga_{0.3}Sb$ buffer cap layer was inserted and a number of additional thin layers were grown to form an InAs-channel HEMT structure. Detailed rationale regarding each layer insertion, such as the hole barrier, doping plane, and buffer cap, can be found in previous publications [1-4]. A critical aspect of dry

etching is to etch through the thin device epi-layers and to stop in the middle of the $Al_{0.7}Ga_{0.3}Sb$ buffer layer, which is sandwiched by AlSb layers. The etch rate must be well controlled to stop within the 0.3 µm $Al_{0.7}Ga_{0.3}Sb$ buffer cap.

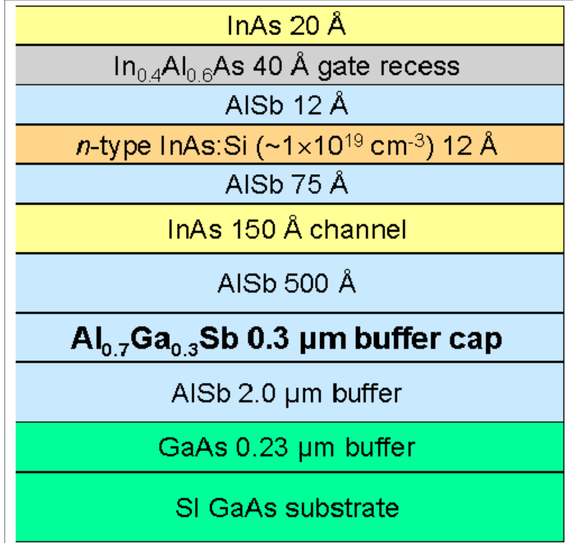

Figure 1. Baseline epitaxial structures.

The wafer fabrication process utilizes qualified InP-HEMT production processes including NGST's 0.1-µm gate E-beam process. Active device mesas were formed by using inductively coupled plasma (ICP) etching with $Cl_2/BCl_3/Ar$ chemistries. Pressure, ICP/Bias power and gas mixture are the main factors that contribute the etching rate. To minimize the possible plasma damage, a low-power condition was selected. At this low-power condition, etch rate studies on GaSb, $Al_{0.7}Ga_{0.3}Sb$ and GaAs samples were conducted utilizing $Cl_2/BCl_3/Ar$ gas chemistries. AlSb and $Al_{0.7}Ga_{0.3}Sb$ layers are the majority of the epitaxial layers that need to be etched. Ideally, etch rate measurement on individual layers would be beneficial for an accurate etch time calculation. However, the AlSb layer was not available because of its high reactivity in air. Thus, the $Al_{0.7}Ga_{0.3}Sb$ layer was selected for calibrating the etch rate. Also, the GaAs and the GaSb layers were selected as reference materials for a etch rate comparison. The etch rate of the $Al_{0.7}Ga_{0.3}Sb$ layer was significantly slower than that of the GaAs layer, while the etch rate of the GaSb was comparable to that of the GaAs. Table 2 summarizes the etch rate comparison of GaSb, $Al_{0.7}Ga_{0.3}Sb$ and GaAs. At 125W/20W ICP/Bias power, 4 mTorr, 2.5 sccm Cl_2/7.5 sccm BCl_3/5 sccm Ar, the etch rate of $Al_{0.7}Ga_{0.3}Sb$ layer was only 110 Å/min, which is about 5 % that of the GaAs and the GaSb layer, at the same process parameters. This suggests that the slower etching rate in the $Al_{0.7}Ga_{0.3}Sb$ layer is attributed to the Al component. BCl_3 gas was found to be more effective for etching $Al_{0.7}Ga_{0.3}Sb$ as compared to Cl_2. The etch rate of $Al_{0.7}Ga_{0.3}Sb$ increased to 160 Å/min from 110 Å/min while the etch rate of both the GaSb and the GaAs significantly decreased by increasing the BCl_3 flow to 10 sccm at the expense of Cl_2 flow. Fig 2 shows the etch rate trends of $Al_{0.7}Ga_{0.3}Sb$ with respect to the Cl_2 percentage in the total gas flow.

Table 2. Etch rate (Å/min) comparison
ICP/Bias Power (125W/20W) and Pressure (4 mT)

Cl_2 %	0 %	25 %
$Al_{0.7}Ga_{0.3}Sb$	160	110
GaSb	1150	2430
GaAs	1050	2330

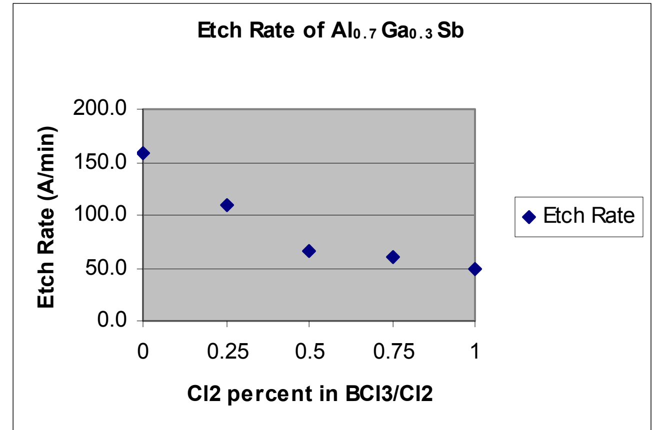

Figure 2. Etch rate of the AlGaSb layer *vs*. Cl_2 percent. ICP Power: 125W, Bias Power: 20W, and Pressure: 4 mT

An optimized process was tested on various target depths into the buffer layer and it was observed that the isolation voltage increased as the etched depth into the $Al_{0.7}Ga_{0.3}Sb$ buffer layer increased as shown

in Figure 3. With an assumption that the leakage current through the surface remains the same, this trend suggests a change of available charges within the $Al_{0.7}Ga_{0.3}Sb$ layer, possibly resulting from its band bending, as the etched depth into the $Al_{0.7}Ga_{0.3}Sb$ layer increases. An average of 100 MΩ/sq of electrical isolation was achieved at the target thickness of 1800 Å.

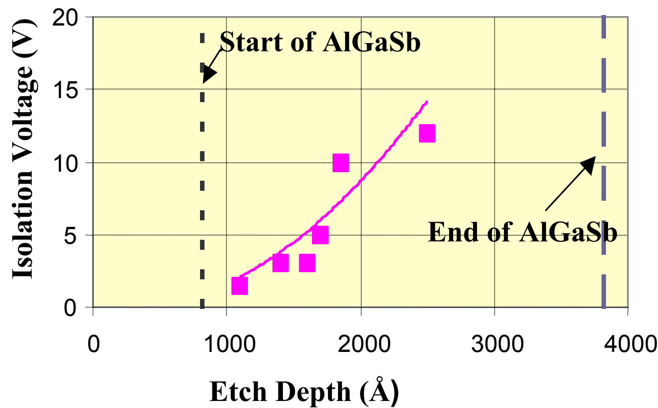

Figure 3. Isolation voltage *vs*. Etched depth.

The smooth mesa floor is highly desirable for integration of various MMIC components such as thin-film resistors. Surface roughness on the mesa floor was evaluated using atomic force microscopy. The dry-etched mesa floor showed rms roughness of 1.67 nm, which is far superior in smoothness as compared to the 15.2 nm from the wet-etched mesa based on acetic and hydrofluoric acid as shown in Figure 4.

The wafers fabricated with Pd/Pt/Au ohmics and electron beam lithography were utilized for 0.1 µm Mo/Au T-gates in a 2 µm source-drain region. The source-to-drain region was 0.8 µm. Other passive circuit components include NiCr thin-film resistors, two levels of interconnect metal including air bridges and a double layer of SiN MIM capacitors. Figure 5 shows the schematics of a circuit cross-section including backside process.

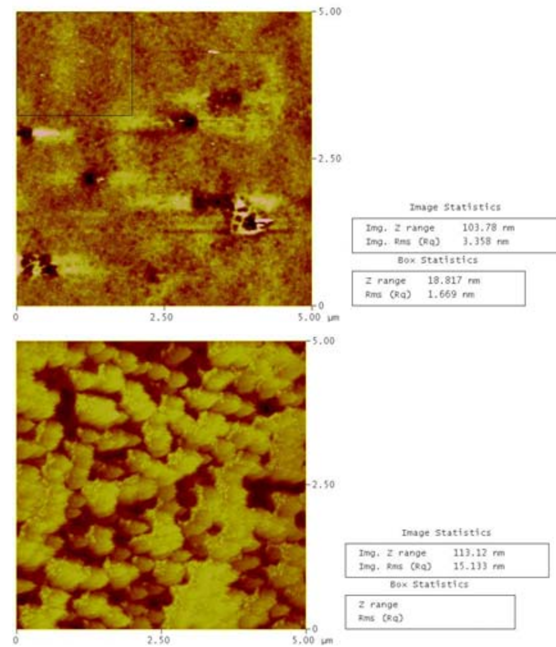

Figure 4. AFM comparison of wet *vs*. dry-etched mesa floors: dry etched (top photo, rms: 1.67 nm), and wet etched (bottom photo, rms: 15.2 nm).

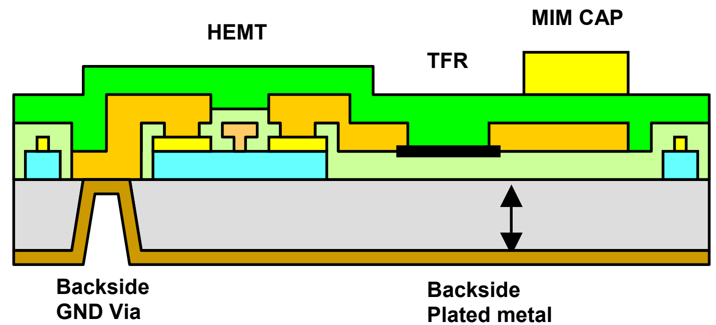

Figure 5. A schematic cross-section of the circuit including backside process.

Devices and Circuits Performance

Small signal RF tests were performed on the wafer fabricated by this shallow mesa isolation technique. The average peak f_T was 160 GHz and 220 GHz at V_{DS} of 0.2 and 0.4 volts and drain current densities of 135 and 340 mA/mm respectively. This shows 5~10 times lower DC power dissipation than a comparable

InP-based HEMT circuit does for the same f_T as shown in Figure 6.

Recently, the first W-Band Low Noise Amplifier (LNA) was demonstrated by utilizing AlSb/InAs HEMT technology [5]. The amplifier operates over an 80-100 GHz bandwidth and demonstrates a minimum noise figure of 5.4-dB with an associated gain of 11.1-dB at an ultra-low total chip dissipation of 1.8-mW. When biased for higher gain, 16 +/- 1 dB is measured over a 77-103 GHz bandwidth, as seen in Figure 7 for a chip dissipation of 4.41-mW.

Table 3. Extrapolated f_T and f_{max}

f_T (GHz)	f_{max} (GHz)	V_{DS} (V)	I_{DS} (mA/mm)	P_{DC} (mW/mm)
220	275	0.5	340	170
160	175	0.2	135	27
82	160	0.1	30	6

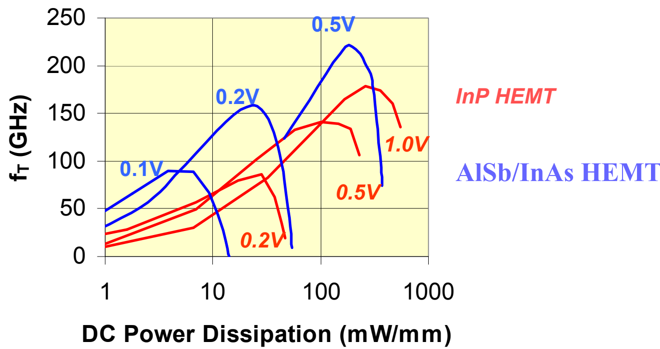

Figure 6. Comparison f_T vs. DC power dissipation.

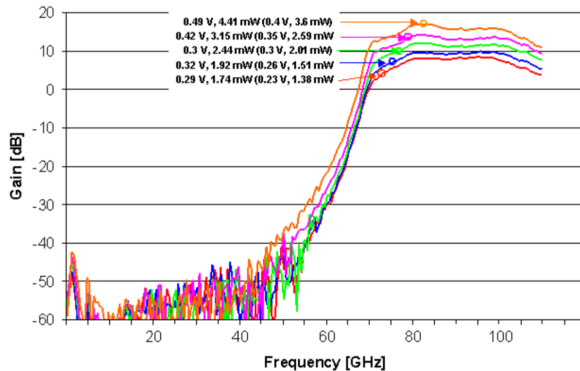

Figure 7. Gain vs. Frequency on W band LNA using AlSb/InAs HEMT.

Conclusions

NGST has developed a shallow mesa isolation for an AlSb/InAs HEMT with an AlGaSb buffer layer by using the inductively coupled plasma etching technique. A controlled etching rate with smooth mesa floor morphology has been demonstated. The resulting devices and circuits demonstrate revolutionary low power dissipation combined with high frequency performance.

Acknowledgements

This work was supported by ONR Cooperative Agreement No.: N00014-01-2-0014, DARPA ABCS Program. The authors would like to thank Don Mullin and Cynthia Hanson (SPAWAR), and Mark Rosker (DARPA).

References

[1] J.B.Boos, et al., IEEE Trans. Electron Device, vol. 45, no. 9, pp. 1869-1875, 1998.

[2] J.B.Boos, et al., Electron Letters, vol. 34, no. 4, pp. 403-404, 1998.

[3] R. Tsai, et al., Proceedings of IEEE Lester Eastman Conf. On High Performance Devices, pp. 276-280, 2002.

[4] R. Tsai. et al., 2004 CS MANTECH Technical Digest, pp.69-72, 2004.

[5] W. Deal et al, Proceedings of GaAs IC Symposium, pp. 301-304, 2004.

ACRONYMS

HEMT: High Electron Mobility Transistor
ICP: Inductively Coupled Plasma
NGST: Northrop Grumman Space Technology
rms: Root Mean Square
LNA: Low Noise Amplifier
MMIC: Monolithic Microwave Integrated Circuit
MIM: Metal Insulator Metal