

# Reliability characterization of high density Metal-Insulator-Metal Capacitors (MIMCAP) fabricated by depositing Silicon Nitride using PECVD in Compound Semiconductor Manufacturing

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## Abstract

**To shrink the size of a die, we have developed high density MIMCAP process for our next generation RFIC products. Using an optimized PECVD process for silicon nitride deposition, we have determined the median time to failure (MTTF) of MIM capacitors using two different electrical tests, Ramp Voltage and Time Dependent Dielectric Breakdown (TDDB). Both of these tests were relatively quick. The TDDB tests required small number of samples. We have compared these lifetimes of MIM capacitors from two different methods at lower operating voltages.**

## INTRODUCTION

In order to shrink the size of a die, one commonly used method is to increase the capacitance density. Capacitors could occupy a very large fraction in die area. The easiest and most cost effective way to increase capacitance density is to decrease the dielectric thickness. As a result of decreasing dielectric thickness, the capacitor breaks down at lower voltages, leading to the possibility of decreased reliability at operating voltages. In this case, a detailed analysis of capacitor reliability in terms of dielectric breakdown is needed. The present study was motivated by this need.

To study dielectric breakdown without extrinsic effects, the capacitor area was kept small. The first method used for studying the reliability of high-density (HD) capacitors was the TDDB test. In a TDDB test setup, a number of identical capacitors are stressed by applying a constant voltage across the two capacitor plates, and the time required for breakdown of each capacitor is determined. From analysis of this life data, the median life is calculated. From measured MTTF data at higher test voltages, the MTTF values at lower operating voltages were projected by using the linear field acceleration model discussed by Berman [1] and Yeats [2]. According to this model, the capacitor life at applied voltage  $V$ :

$$t(V) \propto \exp[-\gamma V] \quad (1)$$

where  $\gamma$  is called the linear field acceleration parameter.

Apart from the TDDB technique, another commonly used method we used for studying capacitor life is called ramp voltage test discussed in references above. The ramp voltage test is based on linear field acceleration model. The incremental time for failure at a desired voltage ( $V$ ) is projected from incremental time for failure at test voltage ( $V_1$ ) by using equation:

$$\Delta t(V, T) = \Delta t(V_1, T_1) \cdot \chi[V, V_1; T, T_1] \quad (2)$$

where

$$\chi[V, V_1; T, T_1] = \exp[-\gamma \cdot (V - V_1)/d + E_a \cdot (1/T - 1/T_1)/k_B] \quad (3)$$

$T_1$  is the temperature in test environment,  $T$  is the temperature of desired environment,  $d$  is the film thickness,  $E_a$  is the activation energy and  $k_B$  is the Boltzman constant.

To determine median life at  $V$  by using equation (2), we need to determine the field acceleration parameter  $\gamma$  in equation (3) above.  $\gamma$  is determined by measuring the breakdown voltages,  $V_{b1}$  and  $V_{b2}$ , at two ramp rates,  $R_{g1}$  and  $R_{g2}$  respectively, both measured at the temperature of the test environment  $T_1$ . In this case,  $\gamma$  is given by equation:

$$\gamma(T_1) = d \cdot \ln(R_{g1}/R_{g2}) / (V_{b1} - V_{b2}) \quad (4)$$

## EXPERIMENTAL

Plasma enhanced CVD process was used for silicon nitride deposition with targeted capacitance densities of about  $0.7\text{fF}/\mu\text{m}^2$  (HD-1), and  $1.2\text{fF}/\mu\text{m}^2$  (HD-2) on 150mm GaAs wafers. The bottom capacitor plate was formed with plated gold, and the top plate was also formed by plated gold. A design of experiments was used for getting the best across wafer capacitance uniformity and maximum capacitor breakdown voltage. Silane to ammonia ratio, deposition pressure and high frequency as well as low frequency RF power were varied to obtain this optimum process condition. The preconditioning of deposition system was also used to minimize run-to-run and lot-to-lot variation. Figures 1 and 2 show capacitance and breakdown voltage distribution of more than 4000 HD-1 type capacitors fabricated over an extended period of time. All the tests described in this paper were run at room temperature.

For measuring intrinsic breakdown voltage, small area capacitors were used ranging from  $0.5\text{pF}$  to  $5\text{pF}$  formed on GaAs wafers. Top plates of these capacitors are smaller than the bottom plates. Also, for breakdown voltage measurements, the bottom plate was

grounded and the top plate was connected to the positive terminal of the probe.

For on-wafer Time Dependent Dielectric Breakdown (TDDB) measurements, a special on-wafer monolithic test circuit was fabricated. This eliminated packaging needs and accelerated the testing process needed for routine monitoring of capacitor reliability in production. Schematic diagram of the test circuit is shown and described in Figure 3. TDDB measurements were made applying a voltage within about 10-20V below the average intrinsic breakdown voltage of the dielectric. An HP4145B based test setup was used for on-wafer TDDB measurements. For each voltage, a bank of 15  $5\text{pF}$  capacitors within a die was tested to obtain capacitor life data. For each failed capacitor, there was approximately  $1.5\text{mA}$  of current increase from the test setup. The lifetime data was analyzed to obtain Median Time to Failure (MTTF) for each voltage. The MTTF of capacitors from intrinsic dielectric failure were then extrapolated to lower operating voltages using linear field acceleration model (equation 1).

Ramp voltage measurements were made with  $0.5\text{pF}$  capacitors using an automated probe station. The devices were scanned along a line close to the wafer center going to within 6mm from wafer edge. Slow ramp and fast ramp measurements were made on two adjacent capacitors within a die measuring 16 pairs of capacitors per wafer. The slow and fast ramp rates for these tests were  $0.5\text{V/s}$  and  $4.3\text{V/s}$  respectively. The breakdown voltage was measured at  $100\mu\text{A}$  and breakdown in each test was confirmed to cause catastrophic failure of capacitor.

Finally, the lifetime data from these TDDB tests were compared with data from ramp voltage tests.

## EXPERIMENTAL RESULTS AND DISCUSSION

### A. TDDB Test

Figure 4 show the current trace as a function of time at one of the test voltages. A catastrophic capacitor failure is indicated by discontinuous increase in current by about 1.5mA in this particular test setup. From these lifetime data, the MTTF was calculated at the test voltage. Due to the particular selection of test voltages, these TDDB tests were relatively quick.

Based on MTTF of capacitor banks measured for 3 test voltages, the MTTF at lower operating voltages were predicted. Figure 5 shows the extrapolated MTTF for HD-1 and HD-2 capacitors. The predicted MTTF values from TDDB study at lower operating voltages are shown in the second and fourth columns in Table 1.

### B. Ramp Voltage Test

Figure 6 show breakdown voltages of 0.5pF capacitors for fast and slow ramps at different sites on wafer. From this data and using equation 4, the median value of acceleration parameter  $\gamma$  was found to be 42.1nm/V and 34.8nm/V for HD-1 and HD-2 capacitors respectively. The projected lifetimes at lower operating voltages, predicted from equations 2 and 3, are shown in columns 3 and 5 in Table 1.

Finally, as shown in Table 1, the predicted MTTF values from ramp voltage and TDDB tests are in good agreement for both HD-1 and HD-2 capacitors.

## SUMMARY

A new on-wafer TDDB test methodology has been presented greatly simplifying this test. Both on-wafer TDDB and ramp voltage tests are acceptable methods for

measuring capacitor reliability at regular intervals in production. Both of these tests are relatively quick and provide comparable results. The time required for TDDB test depend on how far the test voltage is below the average breakdown voltage for the capacitor.

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## REFERENCES

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- [2] B. Yeates, *IEEE Trans. Electron Dev.* **45**, p. 939 (1998).

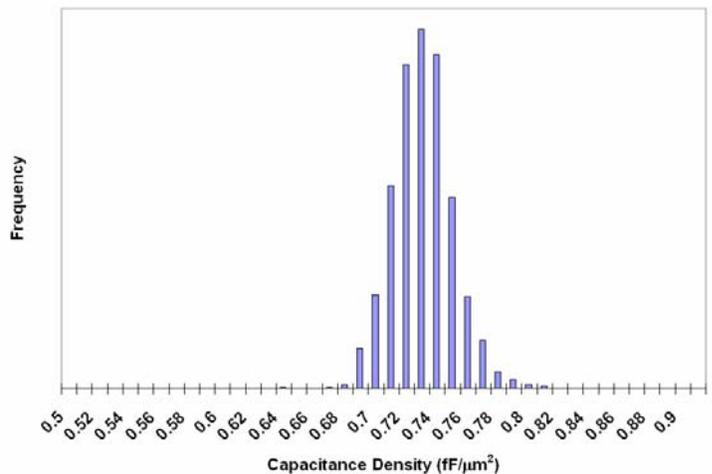


Figure 1. Capacitance density distribution from measurements of over 4000 HD-1 capacitors.

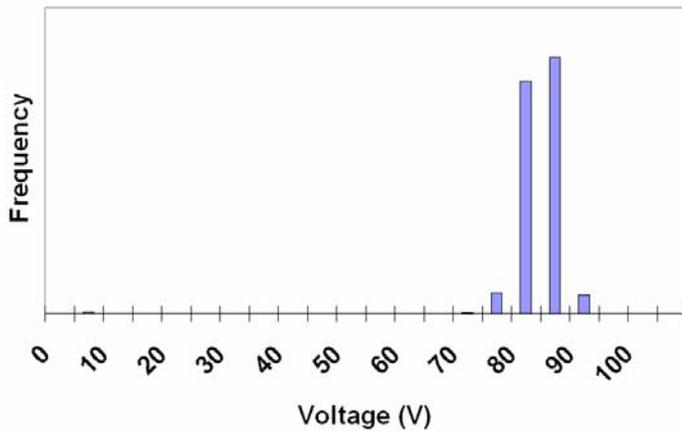


Figure 2. Capacitor breakdown voltage distribution from measurements of over 4000 HD-1 capacitors.

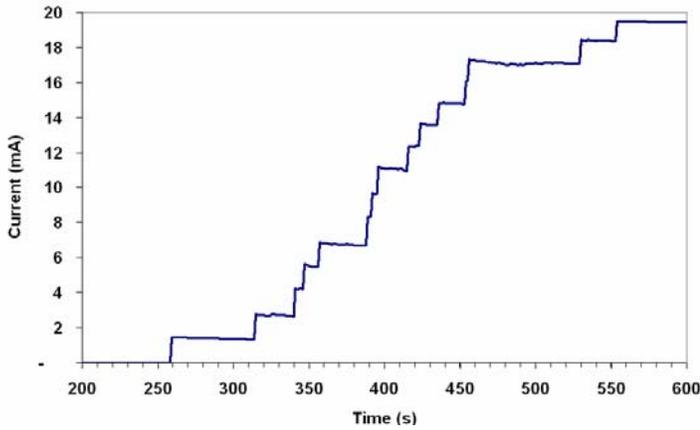


Figure 4. Trace of current from an on-wafer TDDDB test. Current is shown as a function of time showing life of different capacitors in a HD-1 capacitor bank.

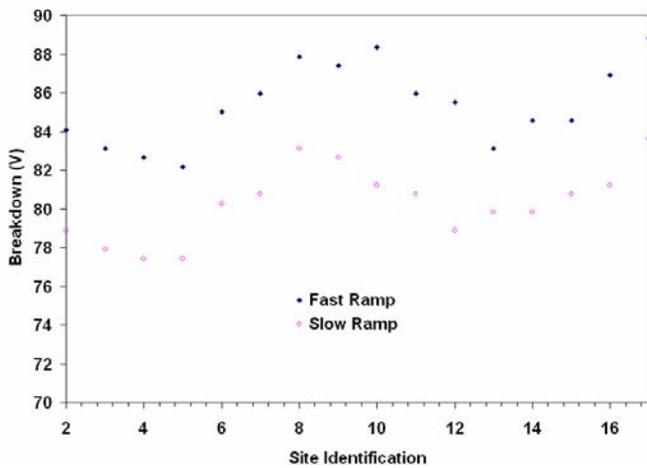


Figure 6. HD-1 capacitor breakdown voltages from ramp voltage tests plotted for different sites.

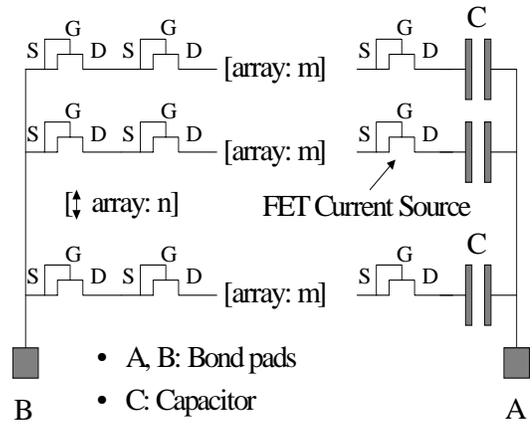


Figure 3. Schematics of capacitor bank structure for on-wafer TDDDB tests. FET chain in a branch carries the stepped up current when the capacitor fails catastrophically. Size  $m$  depends on the range of voltages to be applied across the capacitor plates and the current jump desired. Size  $n$  depends on the area available on die.

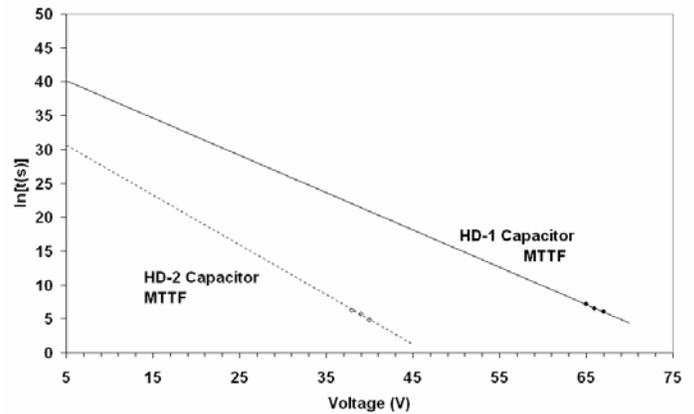


Figure 5. MTTF of HD-1 and HD-2 capacitors at lower operating voltages. These are projected from measured MTTF at higher voltages in TDDDB tests. Time is in units of seconds. Linear field acceleration model was used in these extrapolations.

Voltage	Projected MTTF (hours)			
	HD-1 MIMCAP		HD-2 MIMCAP	
	TDDB	Ramp Voltage	TDDB	Ramp Voltage
15	2.9E+11	2.1E+11	3.6E+06	7.2E+06
10	4.6E+12	2.2E+12	1.4E+08	1.3E+08
5	7.2E+13	2.3E+13	5.7E+09	2.4E+09

Table 1. Predicted HD-1 and HD-2 capacitor MTTF from two different methods compared at 3 voltages.